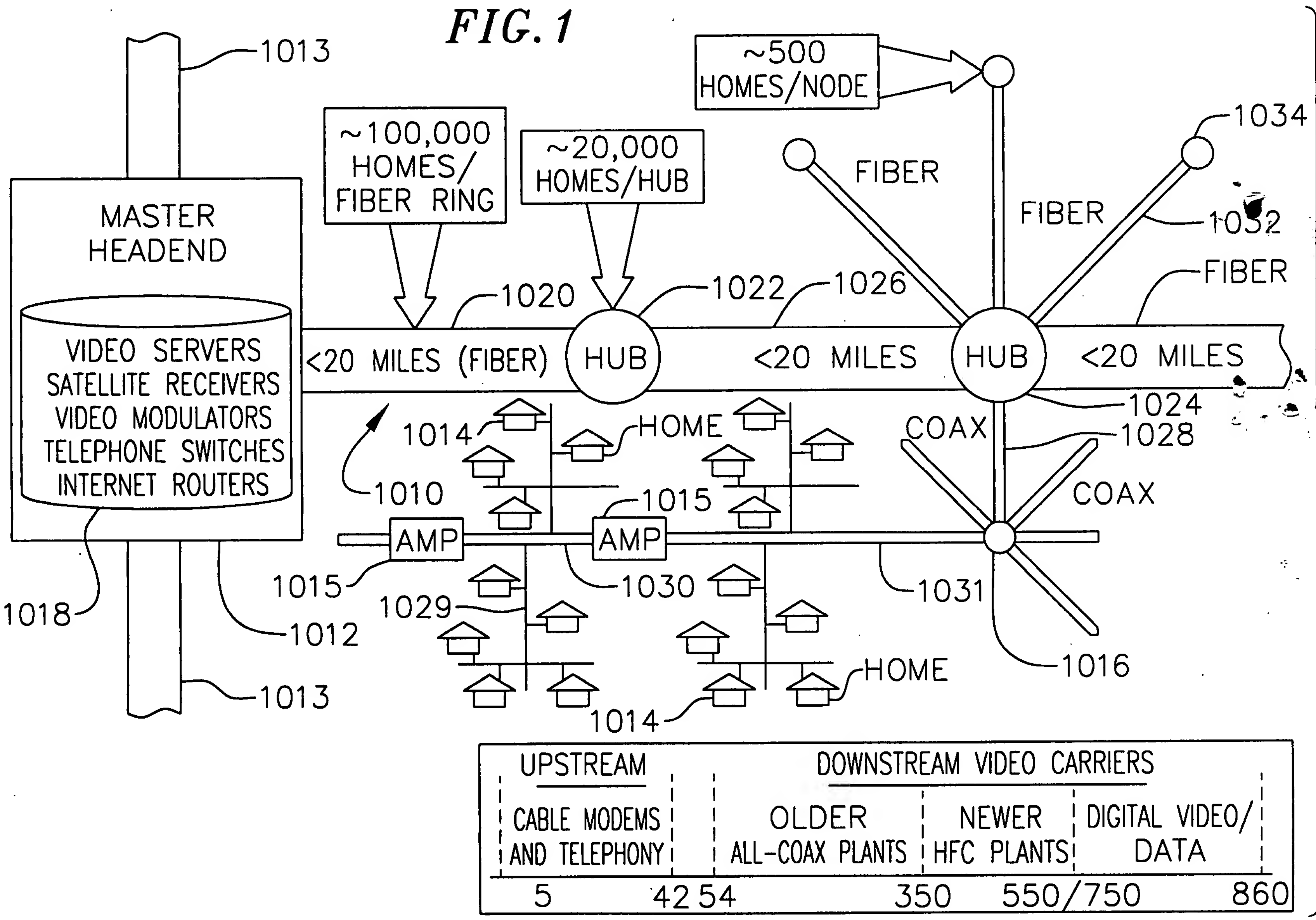
FIG. 1



MASTER HEADEND
VIDEO SERVERS
SATELLITE RECEIVERS
VIDEO MODULATORS
TELEPHONE SWITCHES
INTERNET ROUTERS
1013
1013
1018
1012
~100,000 HOMES/ FIBER RING
~20,000 HOMES/HUB
~500 HOMES/NODE
<20 MILES (FIBER)
HUB
<20 MILES
HUB
<20 MILES
1020
1022
1026
FIBER
FIBER
FIBER
1034
1032
1024
1028
COAX
COAX
1010
1014
HOME
1015
AMP
AMP
1015
1029
1030
1031
1016
HOME
1014
UPSTREAM
CABLE MODEMS AND TELEPHONY
DOWNSTREAM VIDEO CARRIERS
OLDER ALL-COAX PLANTS
NEWER HFC PLANTS
DIGITAL VIDEO/ DATA
5
42
54
350
550/750
860

FIG.2

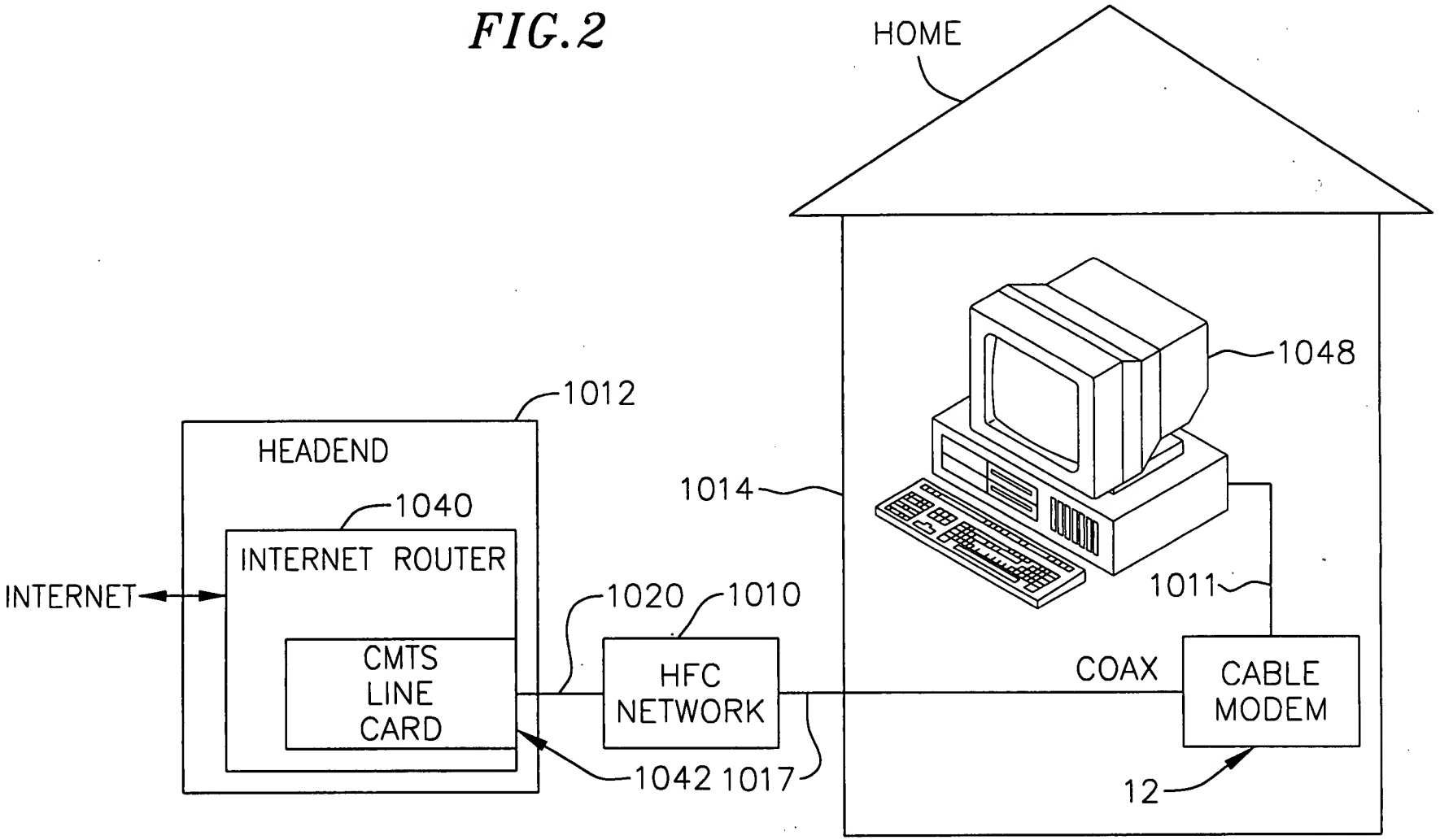

HOME
1048
1012
HEADEND
1014
1040
INTERNET ROUTER
INTERNET
1020
1010
1011
CMTS
LINE
CARD
HFC
NETWORK
COAX
CABLE
MODEM
1042
1017
12

FIG. 3

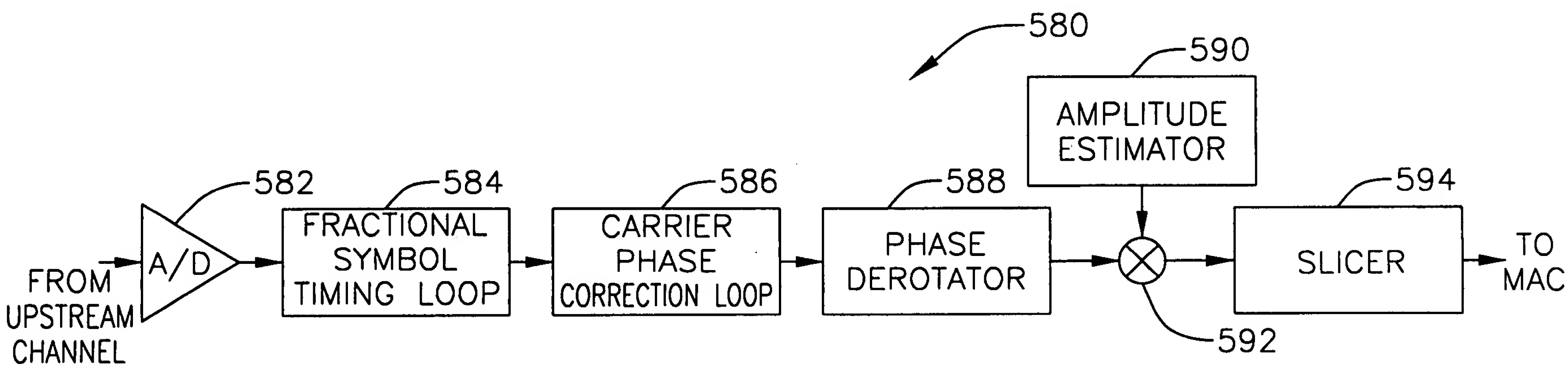

580
FROM
UPSTREAM
CHANNEL
A/D
582
FRACTIONAL
SYMBOL
TIMING LOOP
584
CARRIER
PHASE
CORRECTION LOOP
586
PHASE
DEROTATOR
588
AMPLITUDE
ESTIMATOR
590
592
SLICER
594
TO
MAC

FIG.4

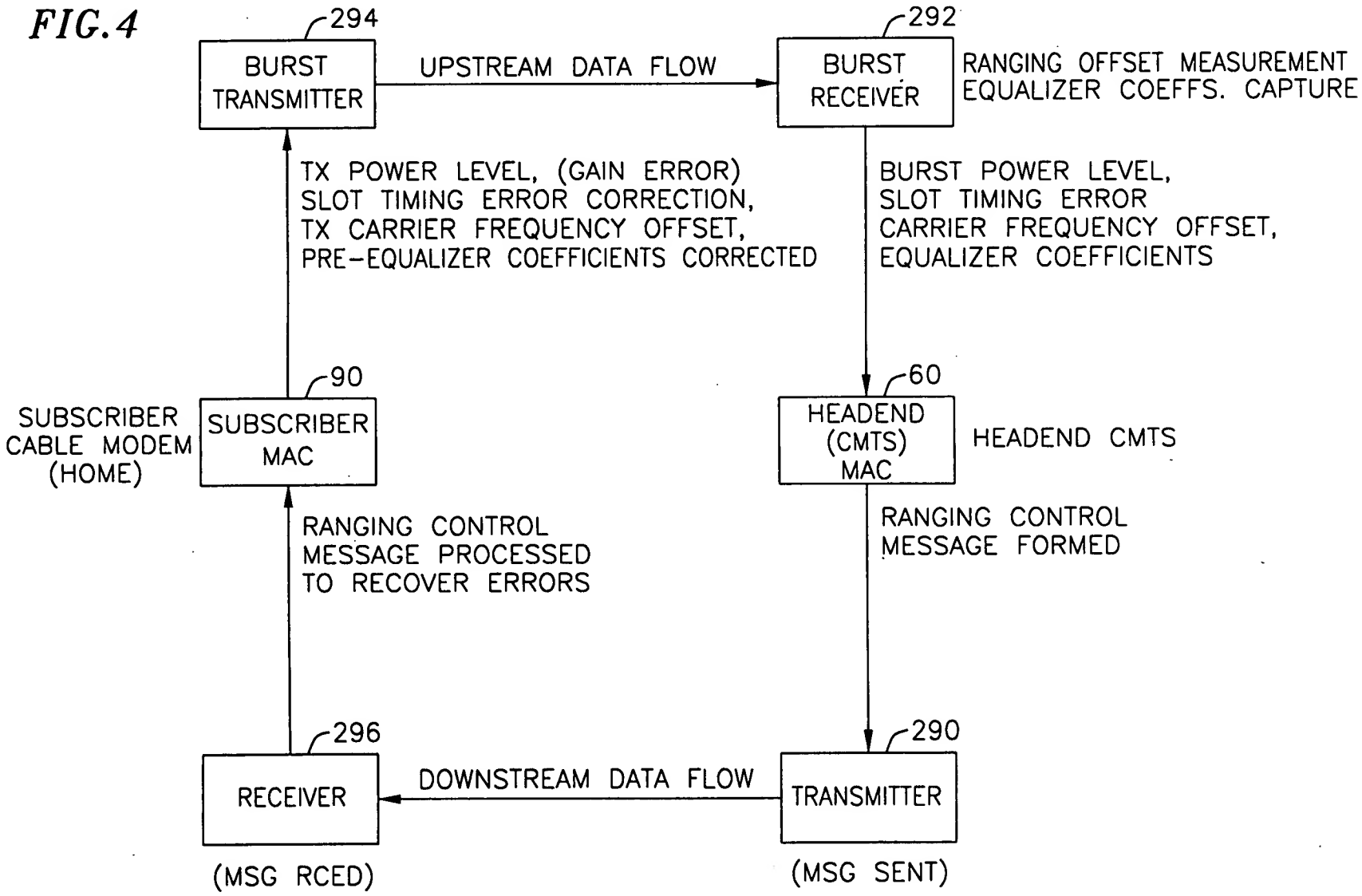
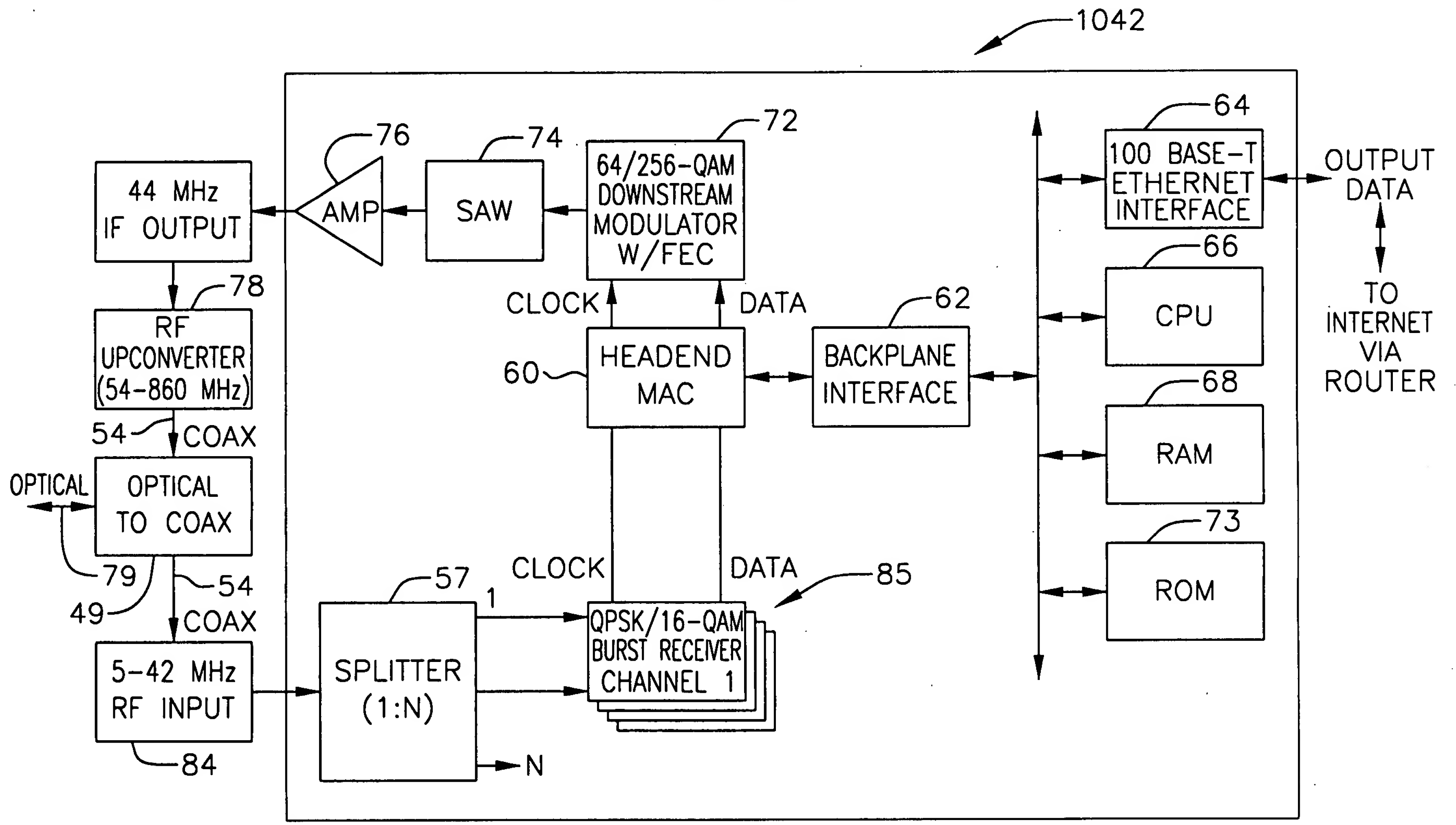

294
BURST TRANSMITTER
UPSTREAM DATA FLOW
292
BURST RECEIVER
RANGING OFFSET MEASUREMENT
EQUALIZER COEFFS. CAPTURE
TX POWER LEVEL, (GAIN ERROR)
SLOT TIMING ERROR CORRECTION,
TX CARRIER FREQUENCY OFFSET,
PRE-EQUALIZER COEFFICIENTS CORRECTED
BURST POWER LEVEL,
SLOT TIMING ERROR
CARRIER FREQUENCY OFFSET,
EQUALIZER COEFFICIENTS
90
SUBSCRIBER CABLE MODEM (HOME)
SUBSCRIBER MAC
60
HEADEND (CMTS) MAC
HEADEND CMTS
RANGING CONTROL
MESSAGE PROCESSED
TO RECOVER ERRORS
RANGING CONTROL
MESSAGE FORMED
296
RECEIVER
DOWNSTREAM DATA FLOW
290
TRANSMITTER
(MSG RCED)
(MSG SENT)

FIG.5A



1042
44 MHz IF OUTPUT
AMP
76
SAW
74
64/256-QAM DOWNSTREAM MODULATOR W/FEC
72
CLOCK
DATA
HEADEND MAC
60
BACKPLANE INTERFACE
62
100 BASE-T ETHERNET INTERFACE
64
OUTPUT DATA
TO INTERNET VIA ROUTER
CPU
66
RAM
68
ROM
73
RF UPCONVERTER (54-860 MHz)
78
54
COAX
OPTICAL
OPTICAL TO COAX
79
49
54
COAX
5-42 MHz RF INPUT
84
SPLITTER (1:N)
57
1
N
CLOCK
DATA
QPSK/16-QAM BURST RECEIVER CHANNEL 1
85

FIG.5B

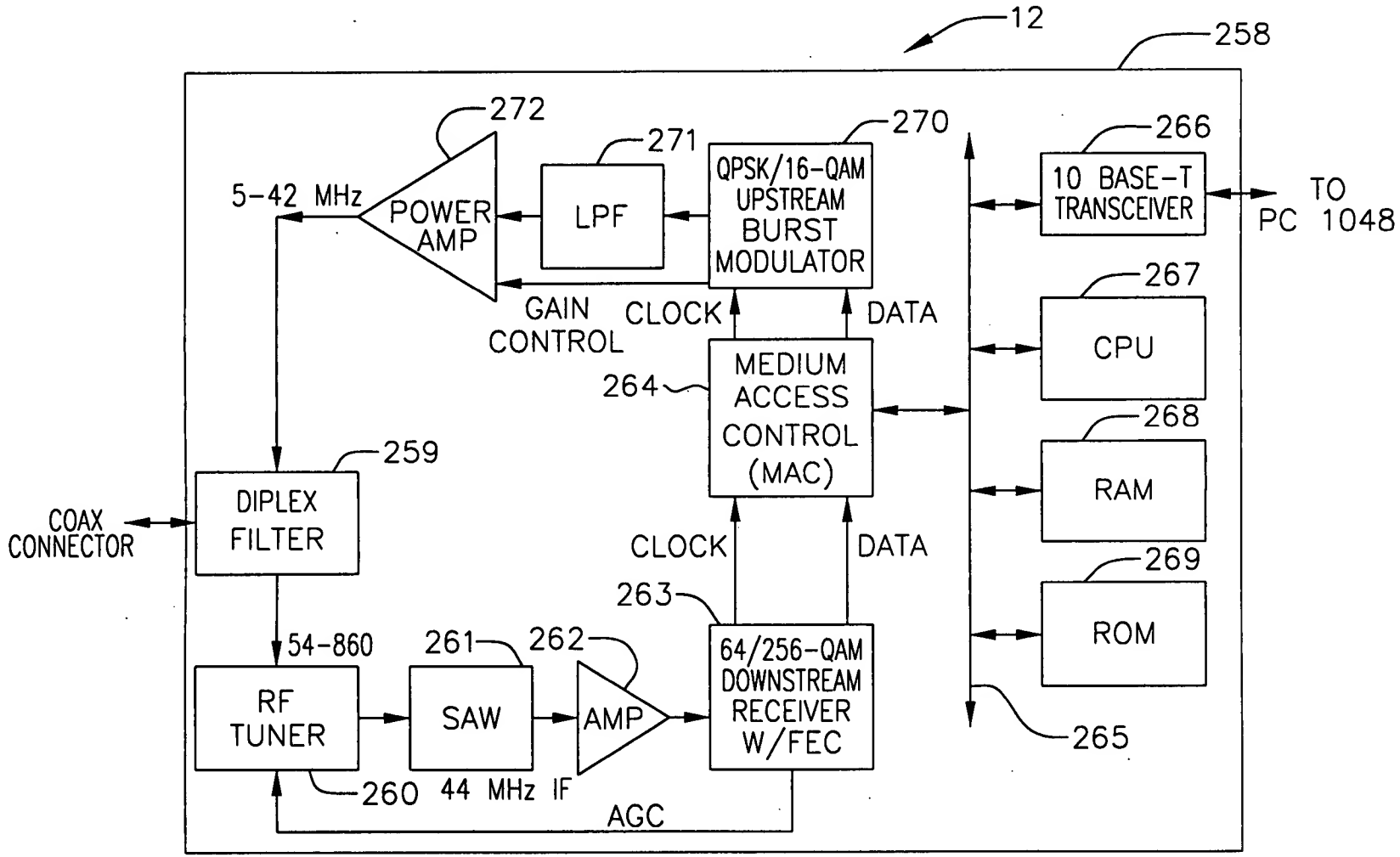

12
258
272
271
270
266
5-42 MHz
POWER AMP
LPF
QPSK/16-QAM UPSTREAM BURST MODULATOR
10 BASE-T TRANSCEIVER
TO PC 1048
GAIN CONTROL
CLOCK
DATA
267
CPU
264
MEDIUM ACCESS CONTROL (MAC)
268
RAM
259
DIPLEX FILTER
COAX CONNECTOR
CLOCK
DATA
269
ROM
263
54-860
261
262
RF TUNER
SAW
AMP
64/256-QAM DOWNSTREAM RECEIVER W/FEC
265
260
44 MHz IF
AGC

FIG.6B

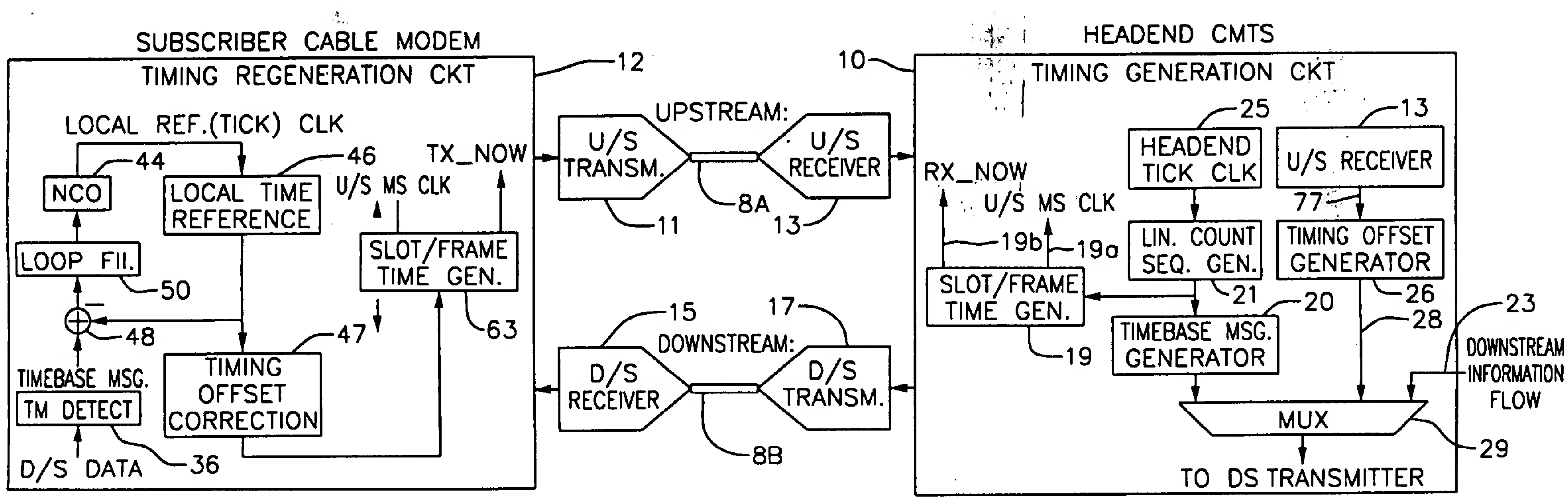
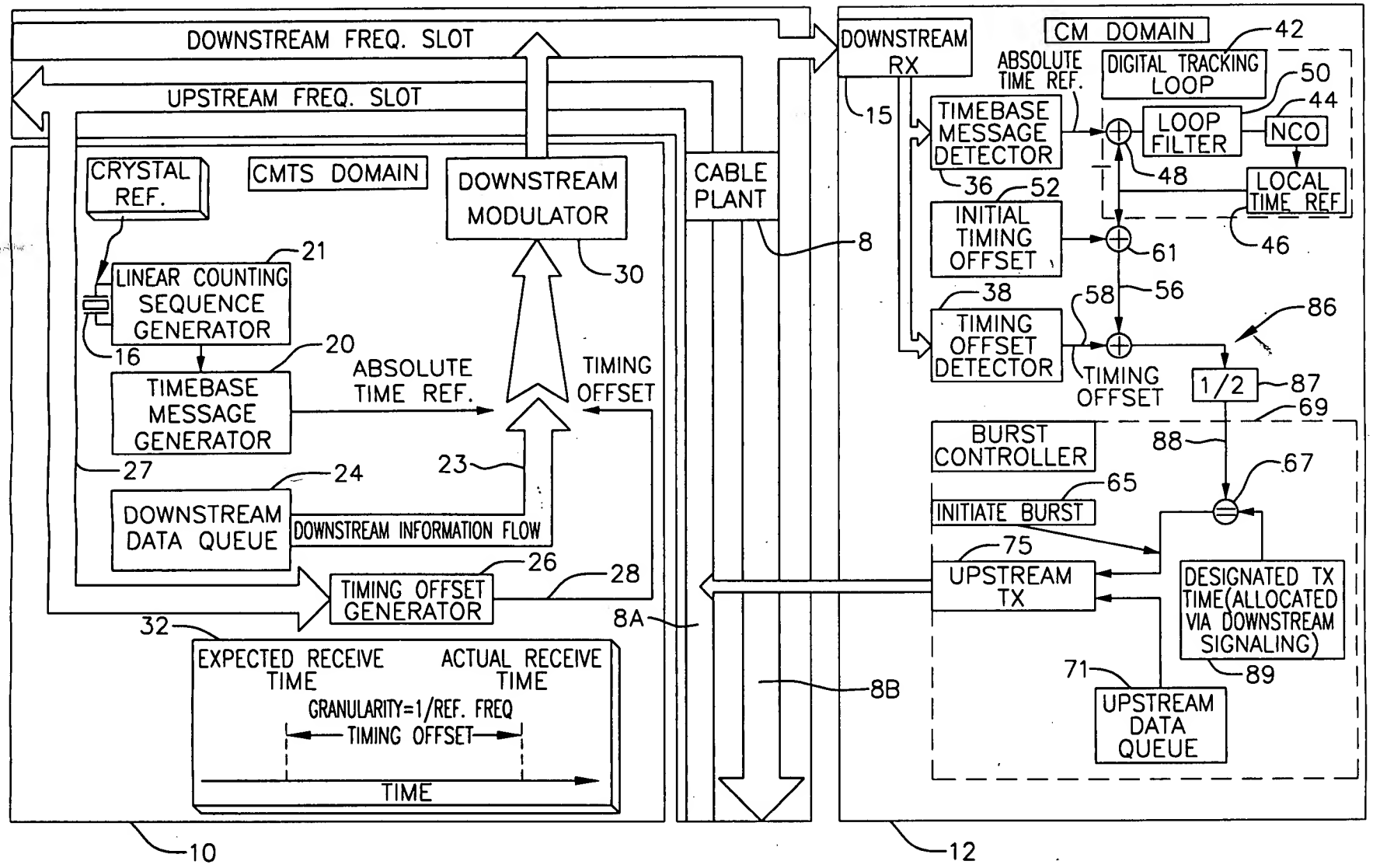

SUBSCRIBER CABLE MODEM
TIMING REGENERATION CKT
LOCAL REF.(TICK) CLK
NCO
44
LOCAL TIME REFERENCE
46
U/S MS CLK
TX_NOW
LOOP FIl.
50
48
TIMEBASE MSG.
TM DETECT
D/S DATA
36
TIMING OFFSET CORRECTION
47
SLOT/FRAME TIME GEN.
63
12
UPSTREAM:
U/S TRANSM.
11
8A
U/S RECEIVER
13
DOWNSTREAM:
D/S RECEIVER
15
8B
D/S TRANSM.
17
10
HEADEND CMTS
TIMING GENERATION CKT
RX_NOW
U/S MS CLK
19b
19a
SLOT/FRAME TIME GEN.
19
HEADEND TICK CLK
25
LIN. COUNT SEQ. GEN.
21
TIMEBASE MSG. GENERATOR
20
U/S RECEIVER
13
77
TIMING OFFSET GENERATOR
26
28
23
DOWNSTREAM INFORMATION FLOW
MUX
29
TO DS TRANSMITTER

FIG. 6A


DOWNSTREAM FREQ. SLOT
UPSTREAM FREQ. SLOT
CRYSTAL REF.
CMTS DOMAIN
DOWNSTREAM MODULATOR
CABLE PLANT
DOWNSTREAM RX
CM DOMAIN
42
ABSOLUTE TIME REF.
DIGITAL TRACKING LOOP
50
44
TIMEBASE MESSAGE DETECTOR
LOOP FILTER
NCO
48
LOCAL TIME REF
36
52
INITIAL TIMING OFFSET
61
46
15
8
21
LINEAR COUNTING SEQUENCE GENERATOR
30
38
58
56
86
16
20
TIMEBASE MESSAGE GENERATOR
ABSOLUTE TIME REF.
TIMING OFFSET
TIMING OFFSET DETECTOR
TIMING OFFSET
1/2
87
69
BURST CONTROLLER
88
67
27
24
23
65
DOWNSTREAM DATA QUEUE
DOWNSTREAM INFORMATION FLOW
INITIATE BURST
75
26
28
UPSTREAM TX
DESIGNATED TX TIME(ALLOCATED VIA DOWNSTREAM SIGNALING)
TIMING OFFSET GENERATOR
8A
32
89
71
EXPECTED RECEIVE TIME
ACTUAL RECEIVE TIME
8B
UPSTREAM DATA QUEUE
GRANULARITY=1/REF. FREQ
TIMING OFFSET
TIME
10
12

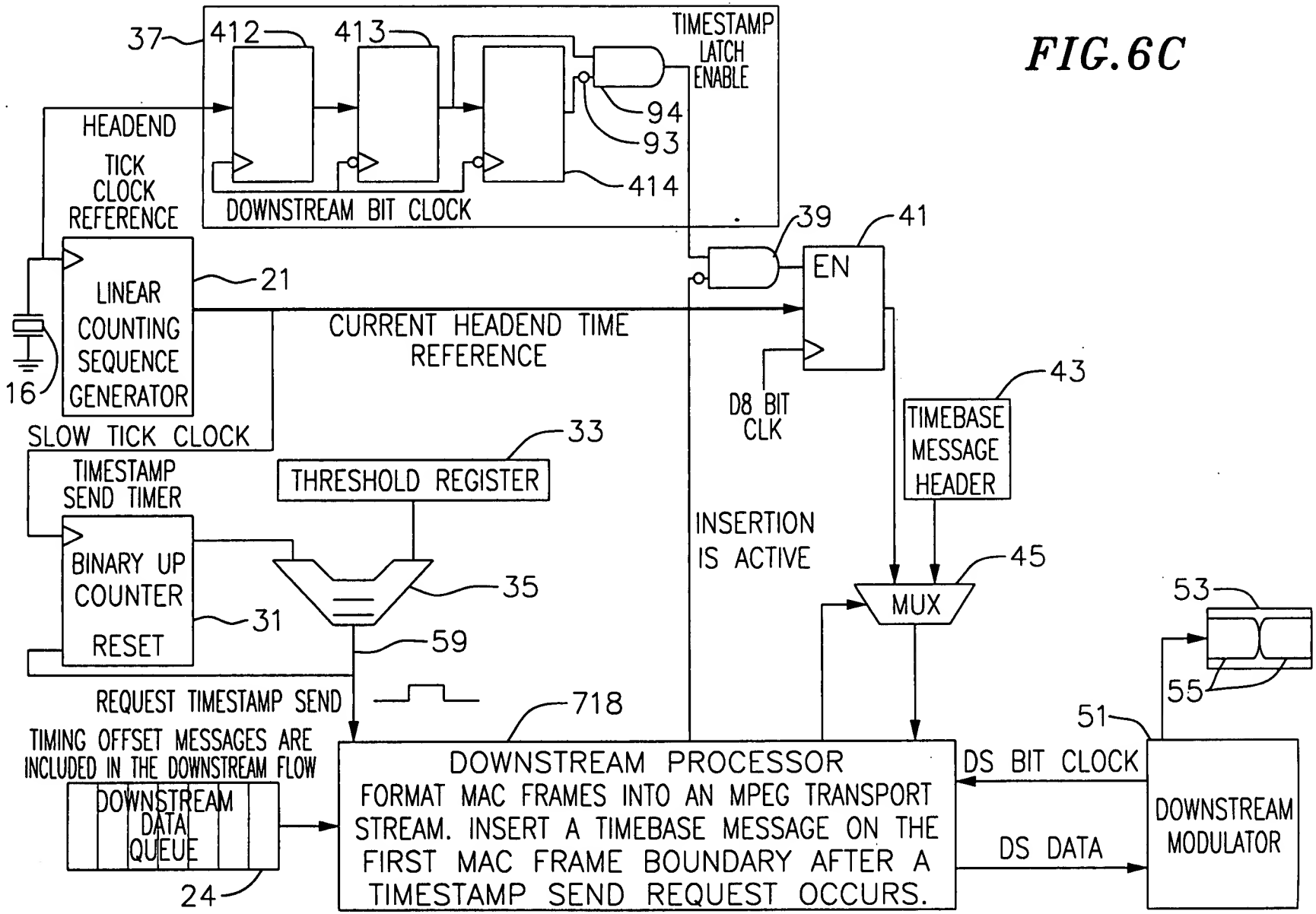

37
412
413
TIMESTAMP LATCH ENABLE
94
93
414
HEADEND TICK CLOCK REFERENCE
DOWNSTREAM BIT CLOCK
39
41
EN
LINEAR COUNTING SEQUENCE GENERATOR
21
16
CURRENT HEADEND TIME REFERENCE
D8 BIT CLK
43
TIMEBASE MESSAGE HEADER
SLOW TICK CLOCK
33
THRESHOLD REGISTER
TIMESTAMP SEND TIMER
BINARY UP COUNTER
RESET
31
35
INSERTION IS ACTIVE
45
MUX
53
55
59
REQUEST TIMESTAMP SEND
718
51
TIMING OFFSET MESSAGES ARE INCLUDED IN THE DOWNSTREAM FLOW
DOWNSTREAM DATA QUEUE
24
DOWNSTREAM PROCESSOR
FORMAT MAC FRAMES INTO AN MPEG TRANSPORT STREAM. INSERT A TIMEBASE MESSAGE ON THE FIRST MAC FRAME BOUNDARY AFTER A TIMESTAMP SEND REQUEST OCCURS.
DS BIT CLOCK
DS DATA
DOWNSTREAM MODULATOR

FIG.6C

FIG. 6D

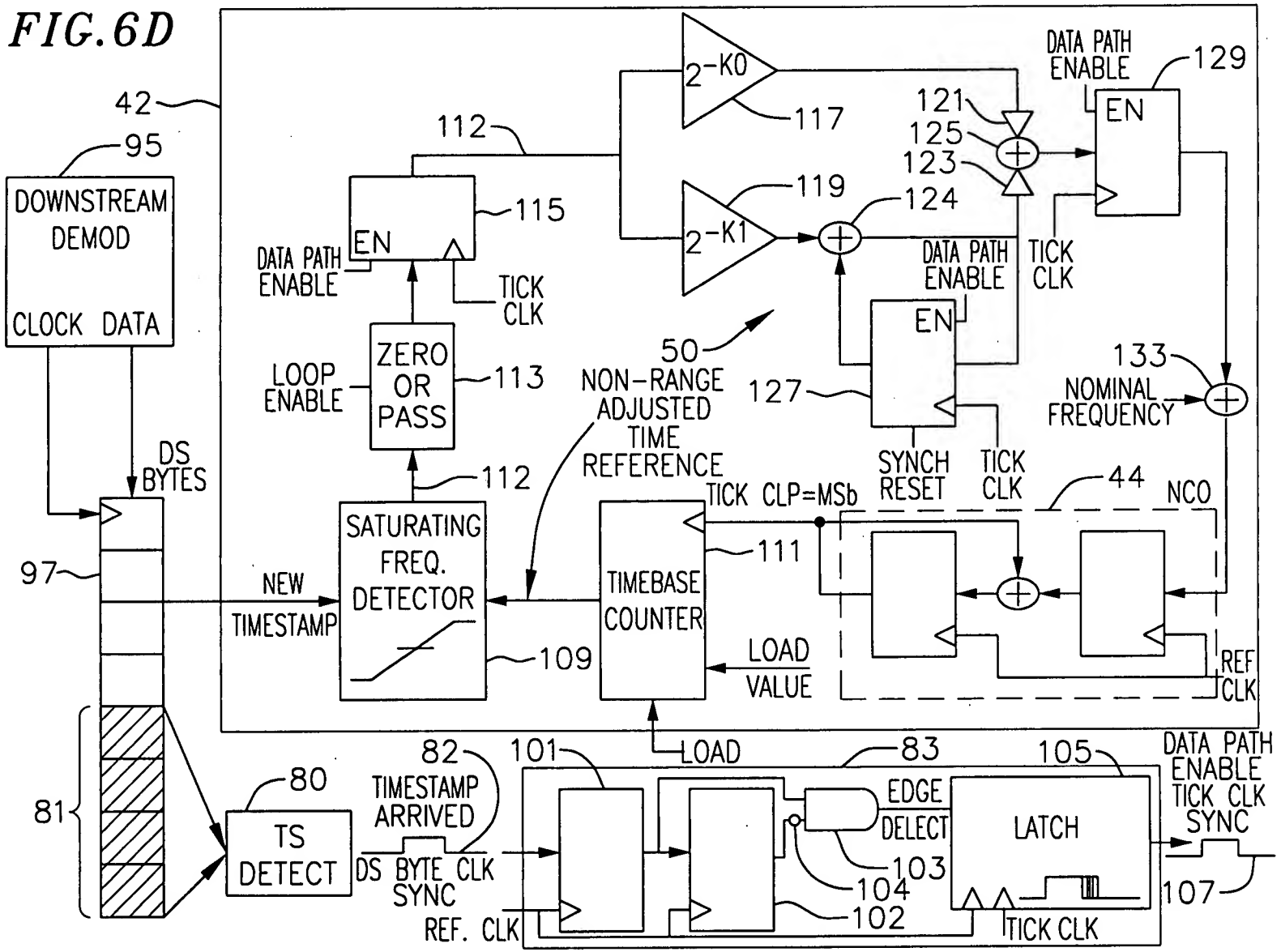

42
95
DOWNSTREAM DEMOD
CLOCK DATA
DS BYTES
97
81
80
TS DETECT
82
TIMESTAMP ARRIVED
DS BYTE CLK SYNC
REF. CLK
112
115
EN
DATA PATH ENABLE
TICK CLK
ZERO OR PASS
LOOP ENABLE
113
112
SATURATING FREQ. DETECTOR
109
NEW TIMESTAMP
NON-RANGE ADJUSTED TIME REFERENCE
50
2-K0
117
2-K1
119
121
125
123
124
DATA PATH ENABLE
129
EN
TICK CLK
EN
127
SYNCH RESET
TICK CLK
133
NOMINAL FREQUENCY
TICK CLP=MSb
TIMEBASE COUNTER
111
LOAD VALUE
LOAD
44
NCO
REF CLK
101
83
105
EDGE DELECT
LATCH
103
104
102
TICK CLK
DATA PATH ENABLE TICK CLK SYNC
107

FIG. 6E

UPDATE RATE	COARSE COEFFS	FINE COEFFICIENTS
1kHz(1ms)	$K0=2^{-11}$ $K1=2^{-15}$ (BW=50Hz)	$K0=2^{-16}$ $K1=2^{-25}$ (BW=1Hz)
300Hz(3.3ms)	$K0=2^{-12}$ $K1=2^{-15}$ (BW=20Hz)	$K0=2^{-16}$ $K1=2^{-23}$ (BW=1Hz)
100Hz(10ms)	$K0=2^{-13}$ $K1=2^{-16}$ (BW=10Hz)	$K0=2^{-16}$ $K1=2^{-22}$ (BW=1Hz)
50Hz(20ms)	$K0=2^{-14}$ $K1=2^{-17}$ (BW=5Hz)	$K0=2^{-16}$ $K1=2^{-21}$ (BW=1Hz)
30Hz(33ms)	$K0=2^{-15}$ $K1=2^{-18}$ (BW=3Hz)	$K0=2^{-17}$ $K1=2^{-21}$ (BW=1Hz)
10Hz(100ms)	$K0=2^{-17}$ $K1=2^{-20}$ (BW=1Hz)	$K0=2^{-17}$ $K1=2^{-20}$ (BW=1Hz)
5Hz(200ms)	$K0=2^{-18}$ $K1=2^{-20}$ (BW=1Hz)	$K0=2^{-18}$ $K1=2^{-20}$ (BW=1Hz)

FIG. 7A

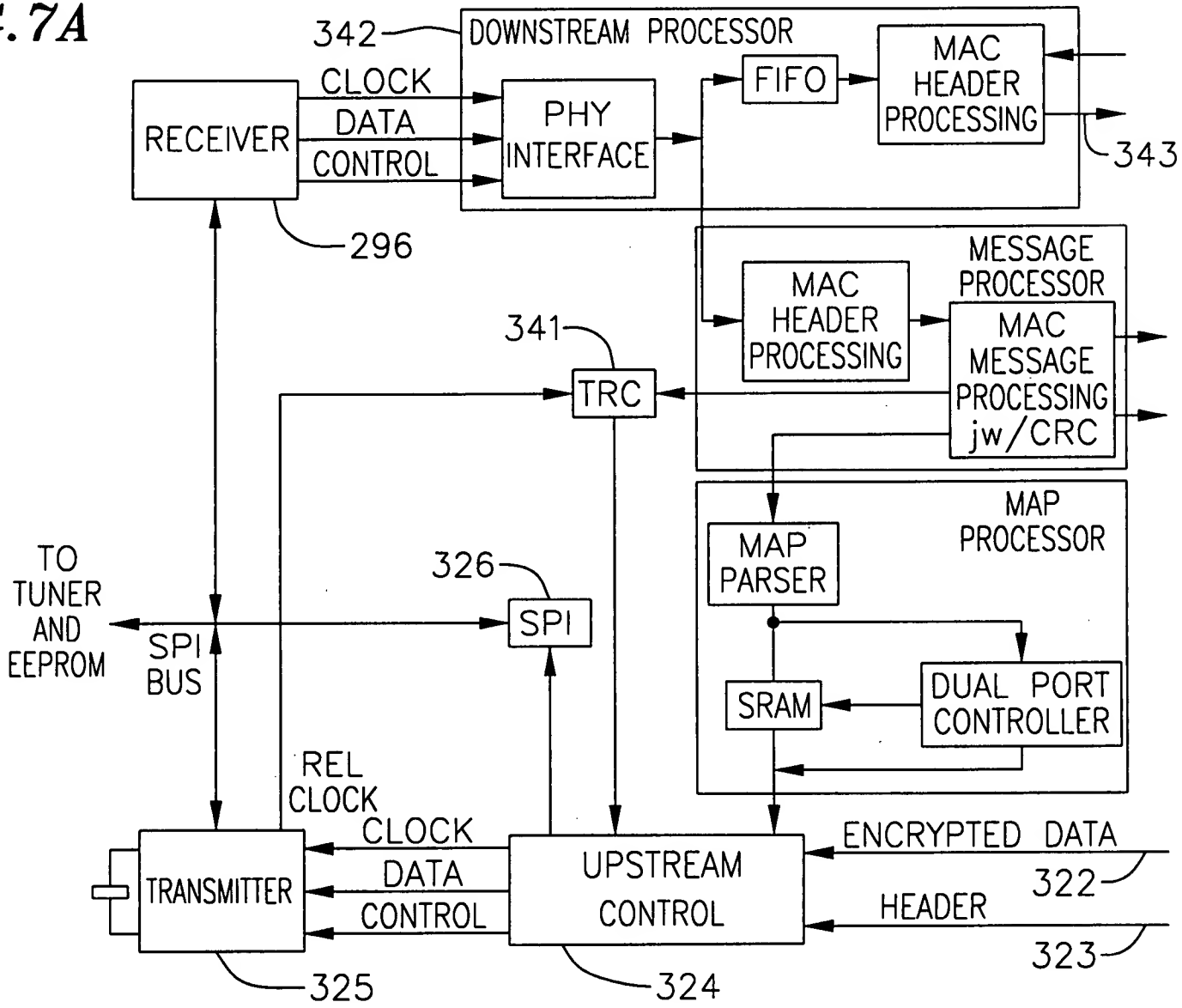
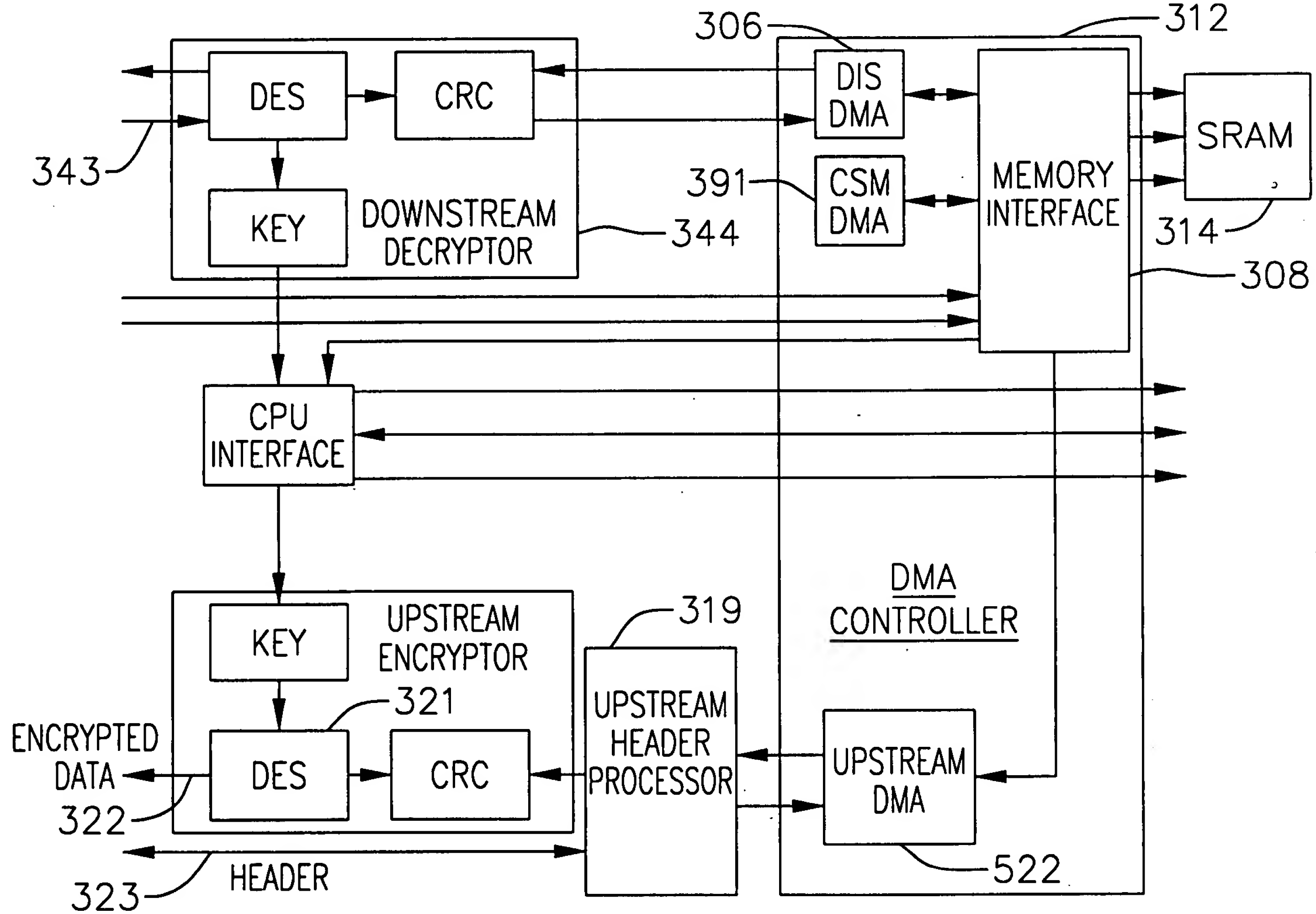

342
DOWNSTREAM PROCESSOR
RECEIVER
CLOCK
DATA
CONTROL
PHY INTERFACE
FIFO
MAC HEADER PROCESSING
343
296
MESSAGE PROCESSOR
MAC HEADER PROCESSING
MAC MESSAGE PROCESSING jw/CRC
341
TRC
MAP PROCESSOR
MAP PARSER
TO TUNER AND EEPROM
326
SPI
SPI BUS
SRAM
DUAL PORT CONTROLLER
REL CLOCK
CLOCK
DATA
CONTROL
TRANSMITTER
UPSTREAM CONTROL
ENCRYPTED DATA
322
HEADER
323
325
324

FIG. 7B



DES
CRC
KEY
DOWNSTREAM DECRYPTOR
343
344
306
DIS DMA
391
CSM DMA
MEMORY INTERFACE
312
SRAM
314
308
CPU INTERFACE
KEY
UPSTREAM ENCRYPTOR
321
DES
CRC
ENCRYPTED DATA
322
HEADER
323
319
UPSTREAM HEADER PROCESSOR
DMA CONTROLLER
UPSTREAM DMA
522

FIG. 8A

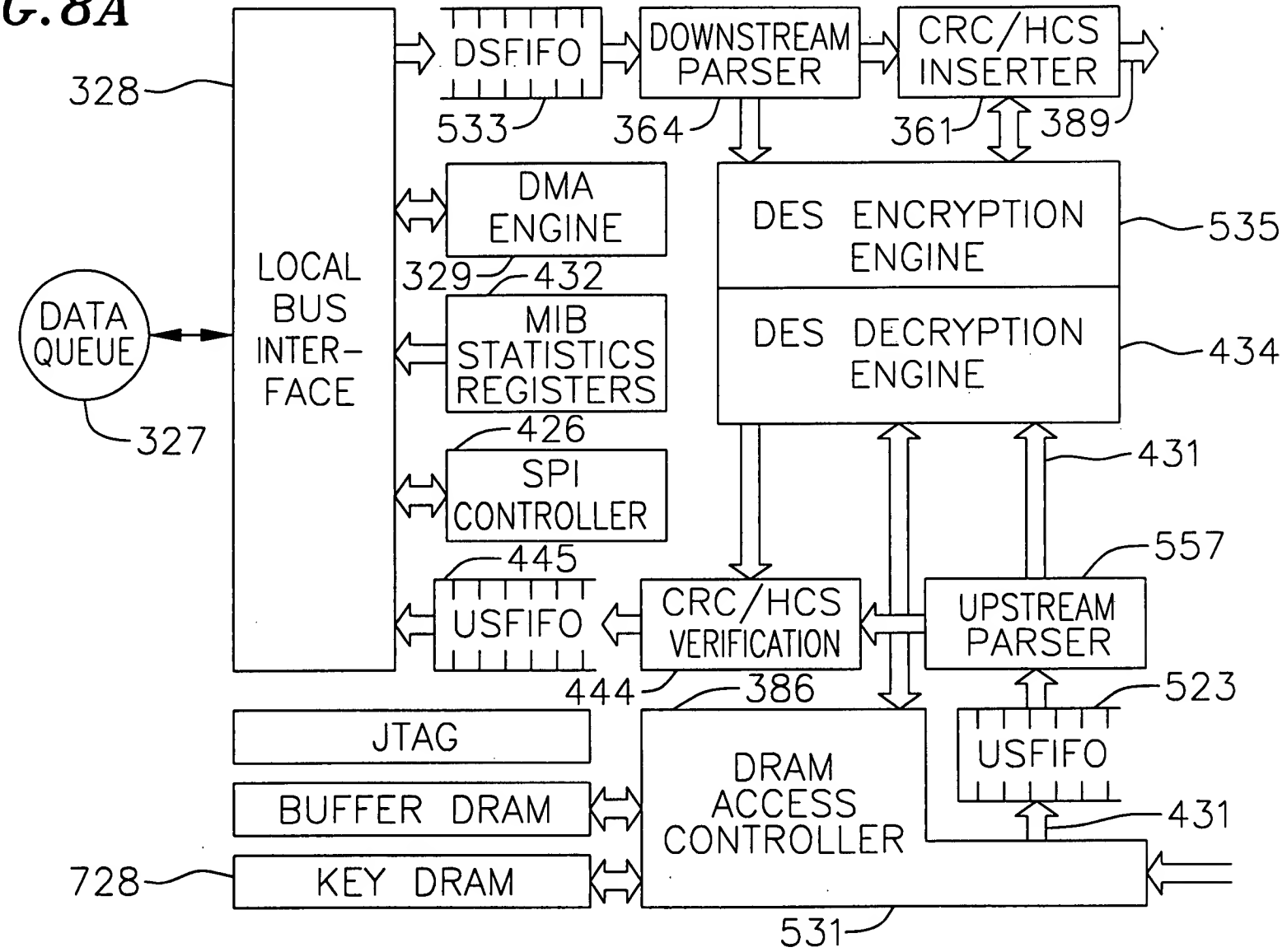
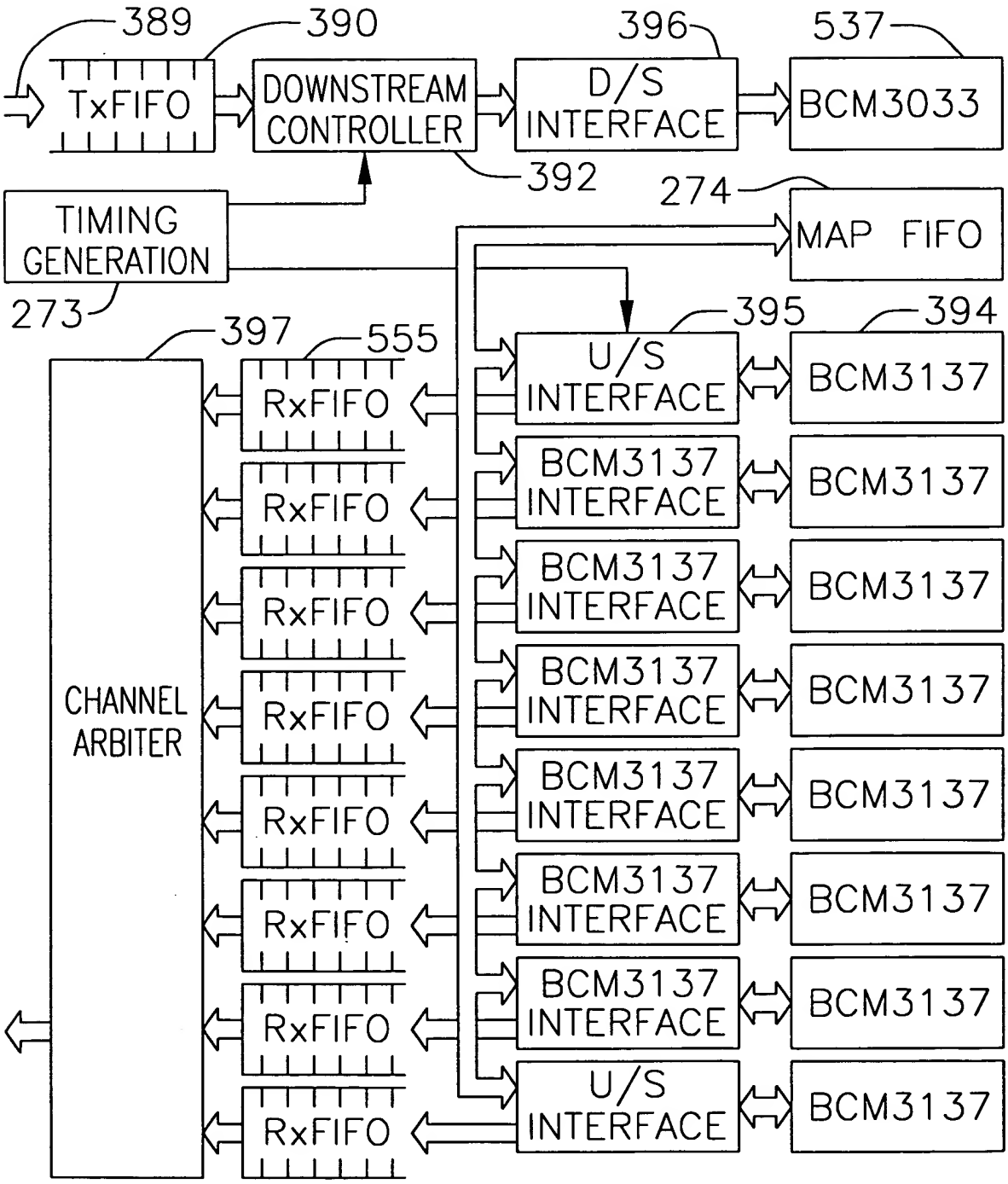
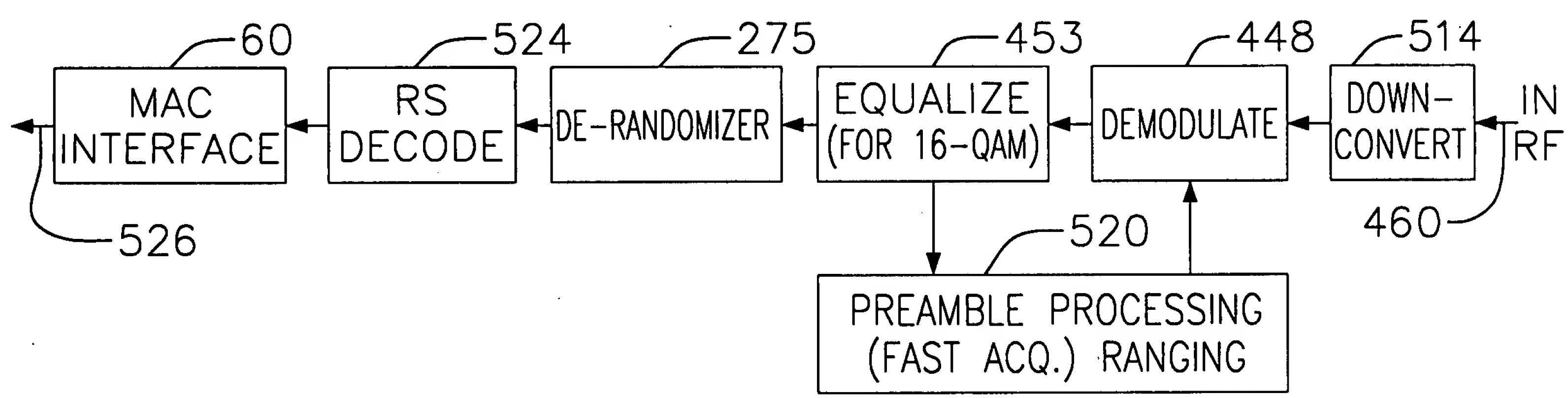

328
LOCAL BUS INTER-FACE
DATA QUEUE
327
DSFIFO
533
DOWNSTREAM PARSER
364
CRC/HCS INSERTER
361
389
DMA ENGINE
329
432
MIB STATISTICS REGISTERS
426
SPI CONTROLLER
445
USFIFO
DES ENCRYPTION ENGINE
535
DES DECRYPTION ENGINE
434
431
557
CRC/HCS VERIFICATION
444
386
UPSTREAM PARSER
523
USFIFO
431
JTAG
BUFFER DRAM
KEY DRAM
728
DRAM ACCESS CONTROLLER
531

FIG.8B


389
390
396
537
TxFIFO
DOWNSTREAM CONTROLLER
D/S INTERFACE
BCM3033
392
274
TIMING GENERATION
MAP FIFO
273
397
555
395
394
U/S INTERFACE
BCM3137
RxFIFO
BCM3137 INTERFACE
CHANNEL ARBITER



60
MAC INTERFACE
524
RS DECODE
275
DE-RANDOMIZER
453
EQUALIZE (FOR 16-QAM)
448
DEMODULATE
514
DOWN-CONVERT
IN RF
460
526
520
PREAMBLE PROCESSING (FAST ACQ.) RANGING

FIG. 9

FIG. 10

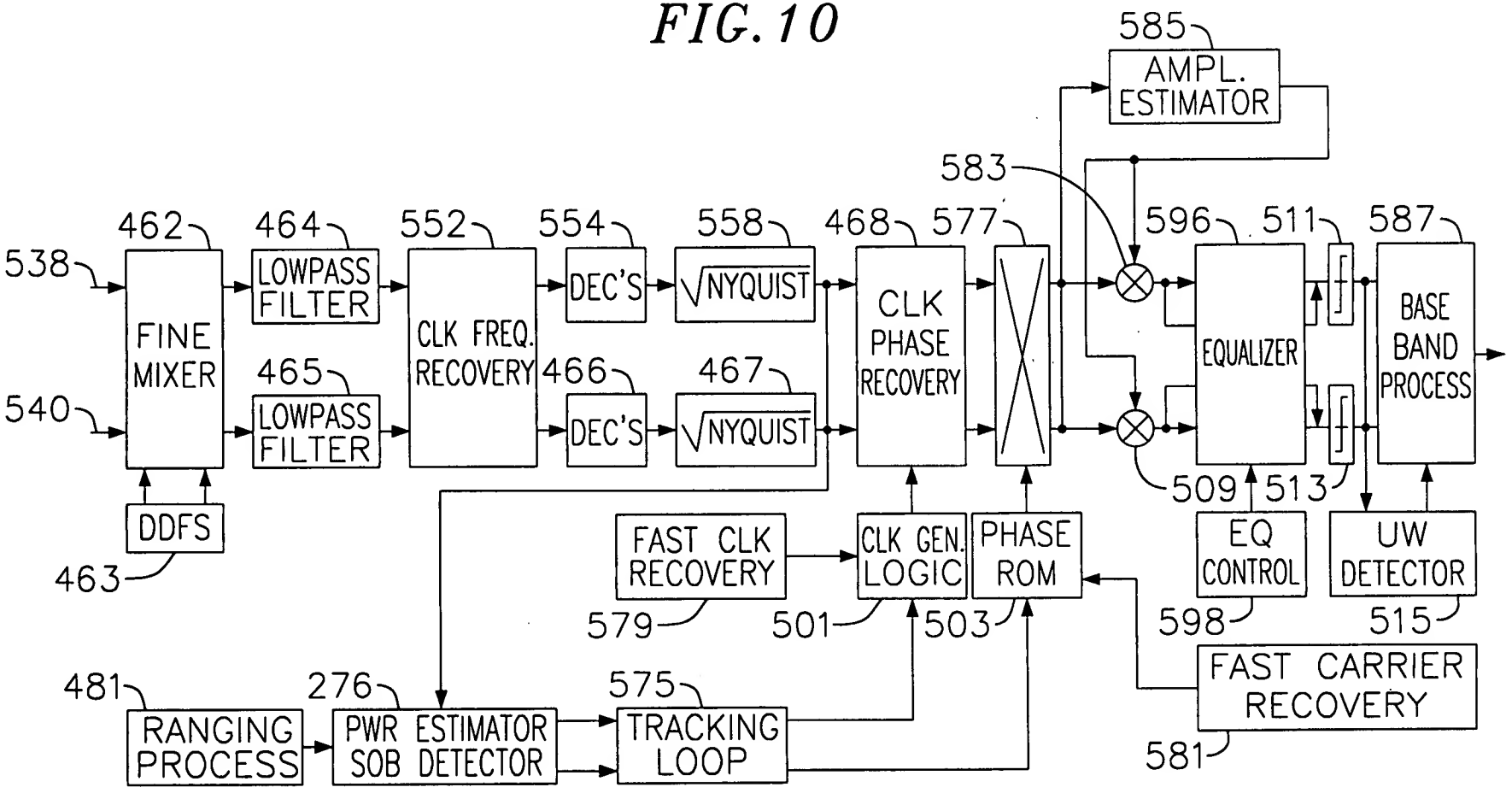

585
AMPL. ESTIMATOR
583
462
464
552
554
558
468
577
596
511
587
538
FINE MIXER
LOWPASS FILTER
CLK FREQ. RECOVERY
DEC'S
√NYQUIST
CLK PHASE RECOVERY
EQUALIZER
BASE BAND PROCESS
540
465
466
467
LOWPASS FILTER
DEC'S
√NYQUIST
509
513
DDFS
463
FAST CLK RECOVERY
CLK GEN. LOGIC
PHASE ROM
EQ CONTROL
UW DETECTOR
579
501
503
598
515
481
276
575
RANGING PROCESS
PWR ESTIMATOR SOB DETECTOR
TRACKING LOOP
FAST CARRIER RECOVERY
581

FIG. 11

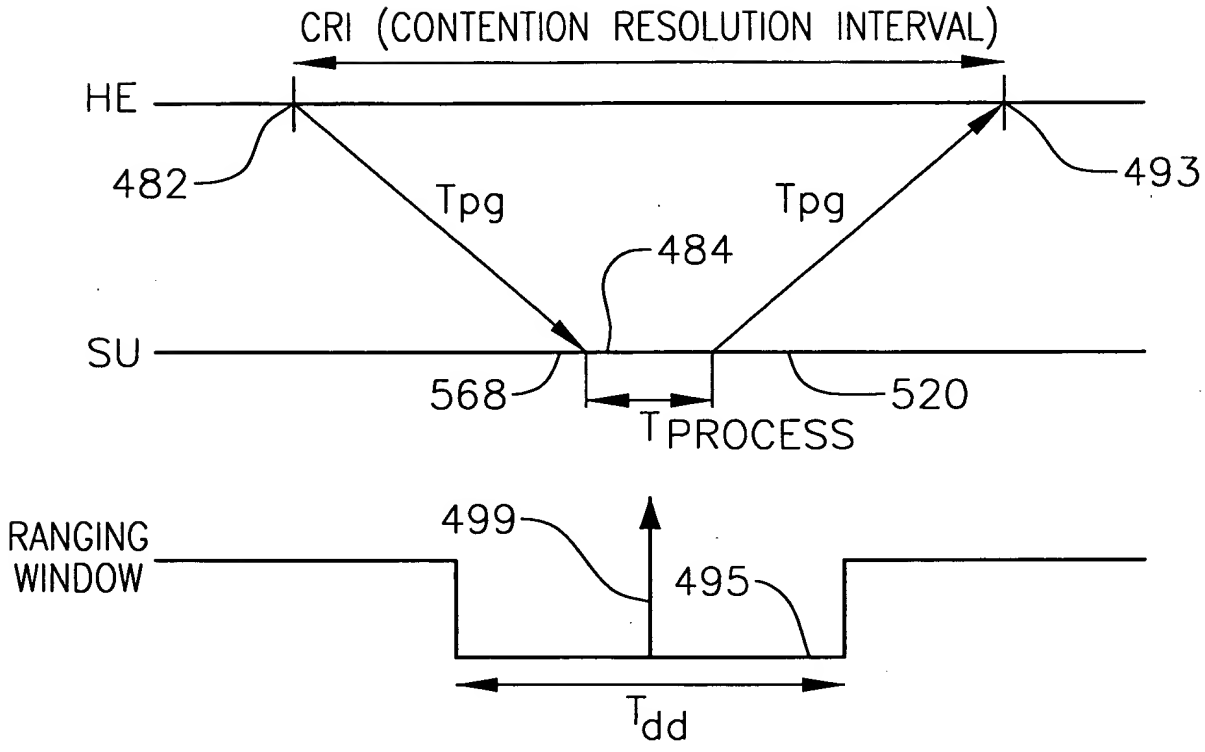

CRI (CONTENTION RESOLUTION INTERVAL)
HE
482
Tpg
Tpg
493
484
SU
568
520
TPROCESS
RANGING WINDOW
499
495
Tdd

FIG. 12

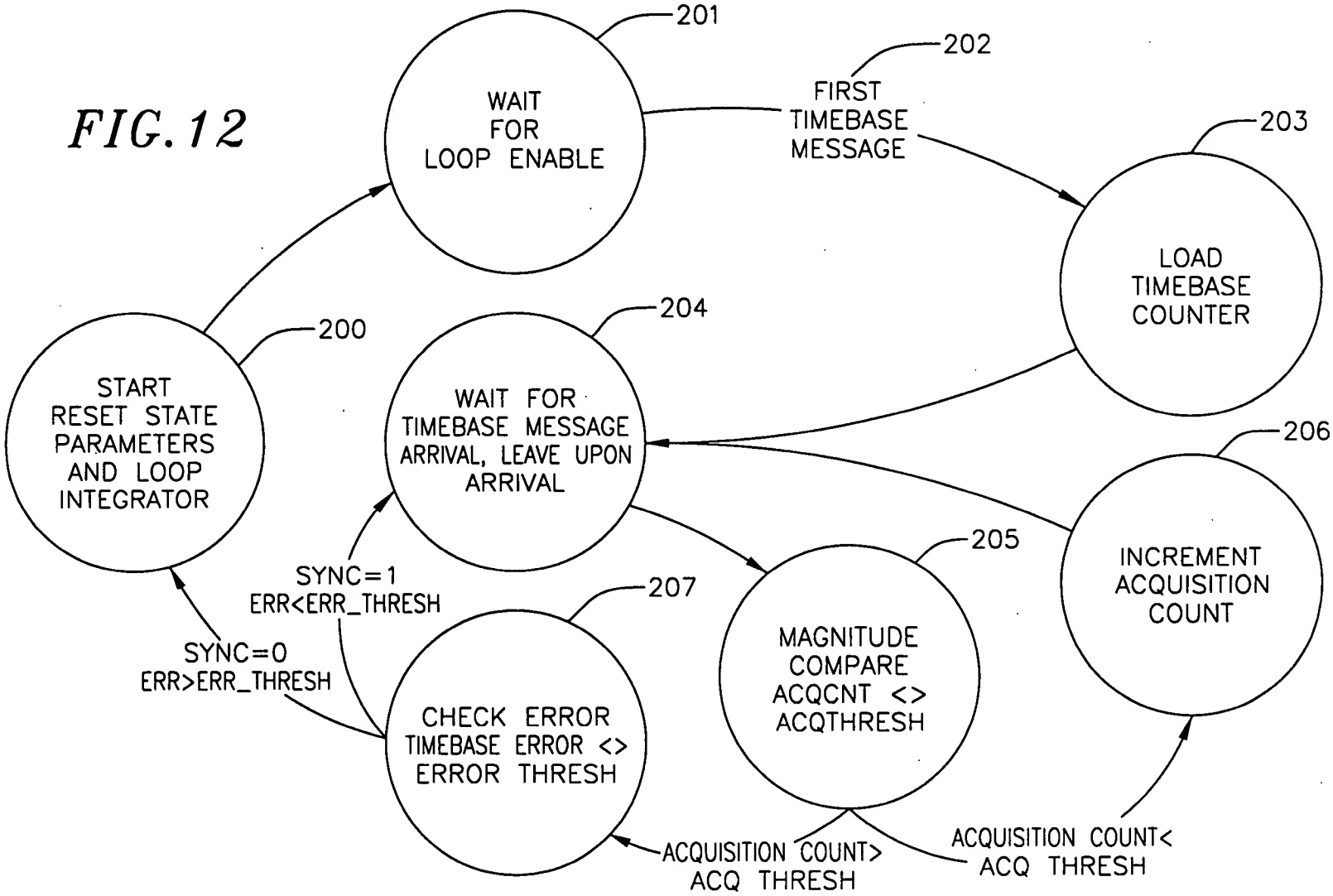

201
WAIT FOR LOOP ENABLE
202
FIRST TIMEBASE MESSAGE
203
LOAD TIMEBASE COUNTER
200
START RESET STATE PARAMETERS AND LOOP INTEGRATOR
204
WAIT FOR TIMEBASE MESSAGE ARRIVAL, LEAVE UPON ARRIVAL
206
INCREMENT ACQUISITION COUNT
205
MAGNITUDE COMPARE ACQCNT <> ACQTHRESH
SYNC=1 ERR<ERR_THRESH
207
SYNC=0 ERR>ERR_THRESH
CHECK ERROR TIMEBASE ERROR <> ERROR THRESH
ACQUISITION COUNT> ACQ THRESH
ACQUISITION COUNT< ACQ THRESH

FIG. 13

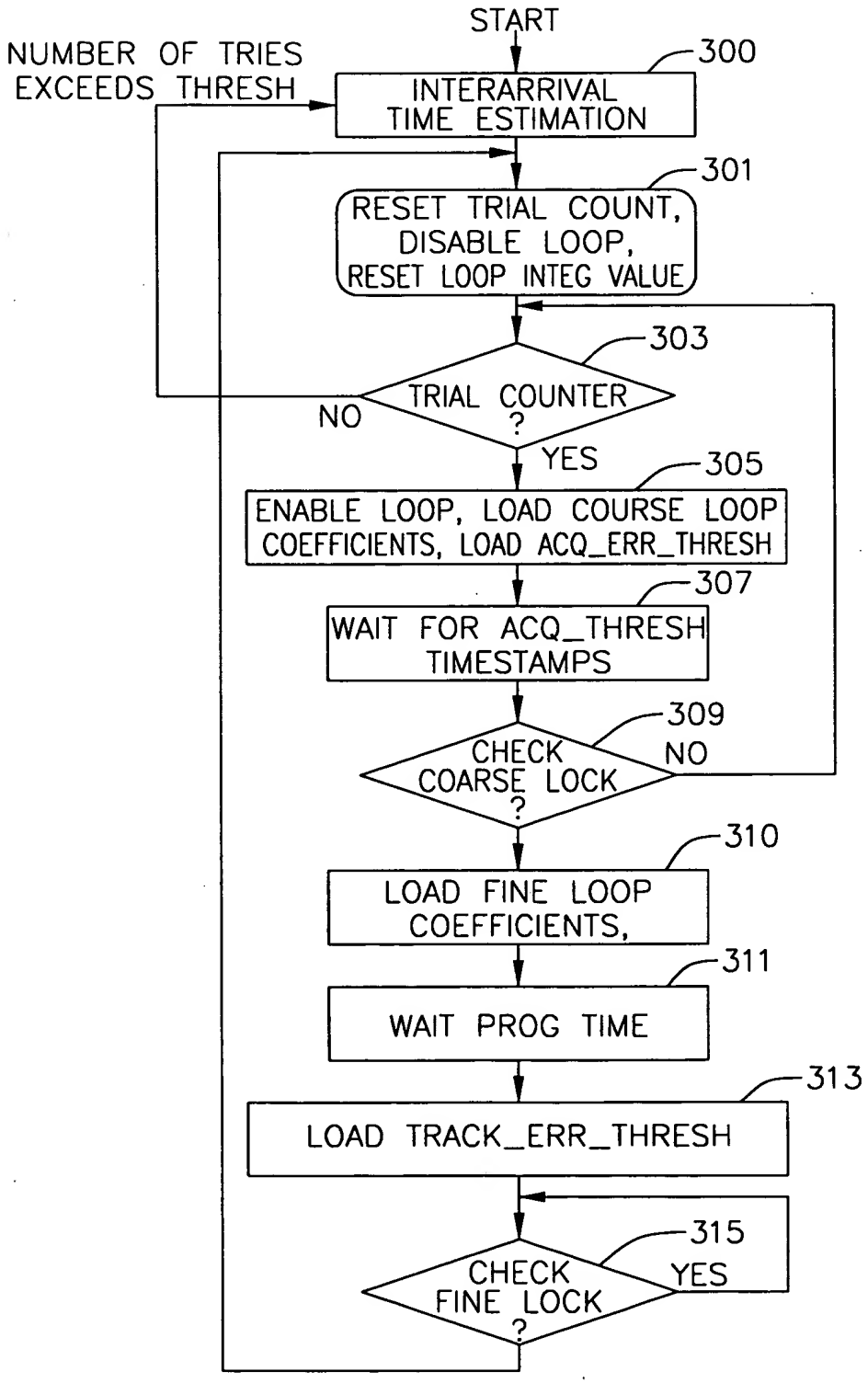

START
NUMBER OF TRIES EXCEEDS THRESH
300
INTERARRIVAL TIME ESTIMATION
301
RESET TRIAL COUNT, DISABLE LOOP, RESET LOOP INTEG VALUE
303
TRIAL COUNTER ?
NO
YES
305
ENABLE LOOP, LOAD COURSE LOOP COEFFICIENTS, LOAD ACQ_ERR_THRESH
307
WAIT FOR ACQ_THRESH TIMESTAMPS
309
CHECK COARSE LOCK ?
NO
310
LOAD FINE LOOP COEFFICIENTS,
311
WAIT PROG TIME
313
LOAD TRACK_ERR_THRESH
315
CHECK FINE LOCK ?
YES

FIG. 14

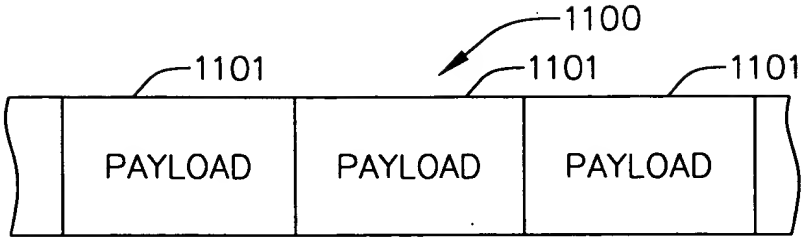


FIG. 15

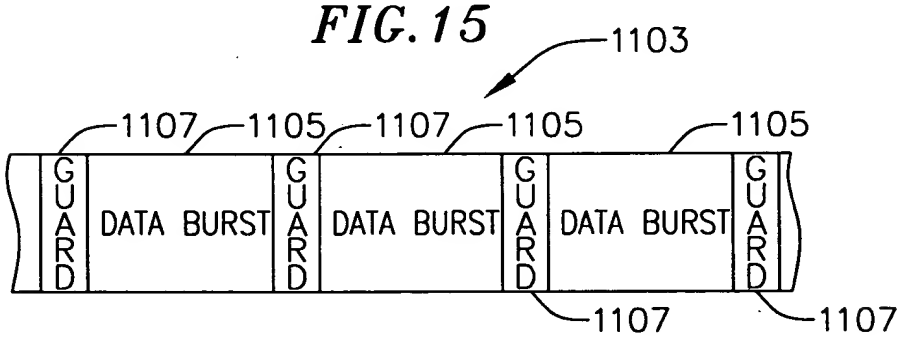


FIG. 16

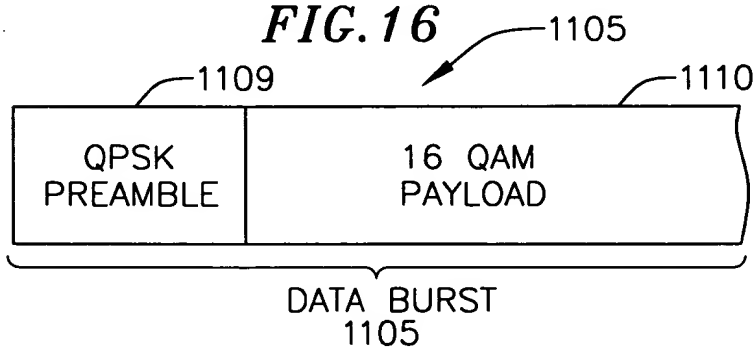


FIG. 17

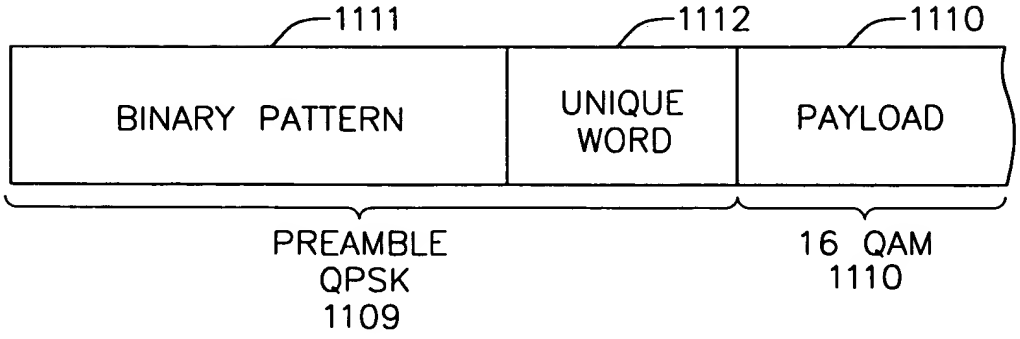


FIG. 18

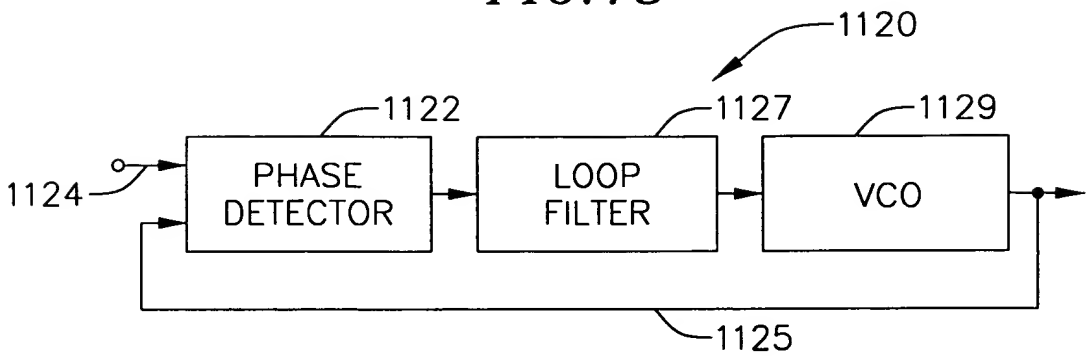


FIG. 19

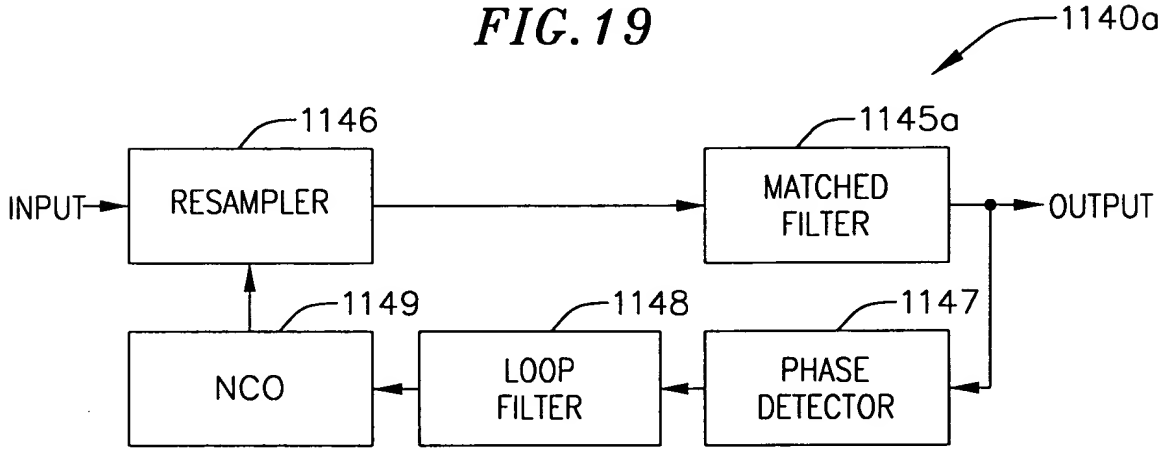


FIG. 20

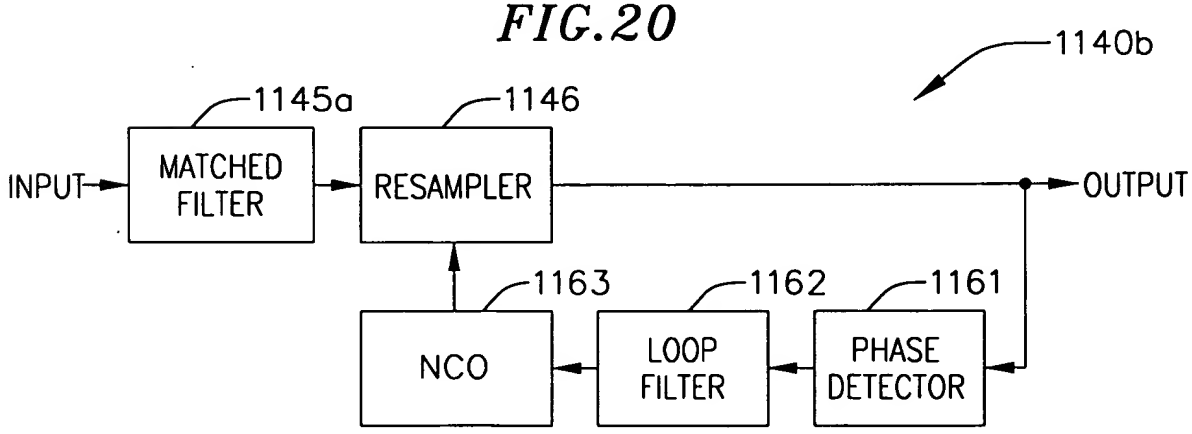


FIG.21

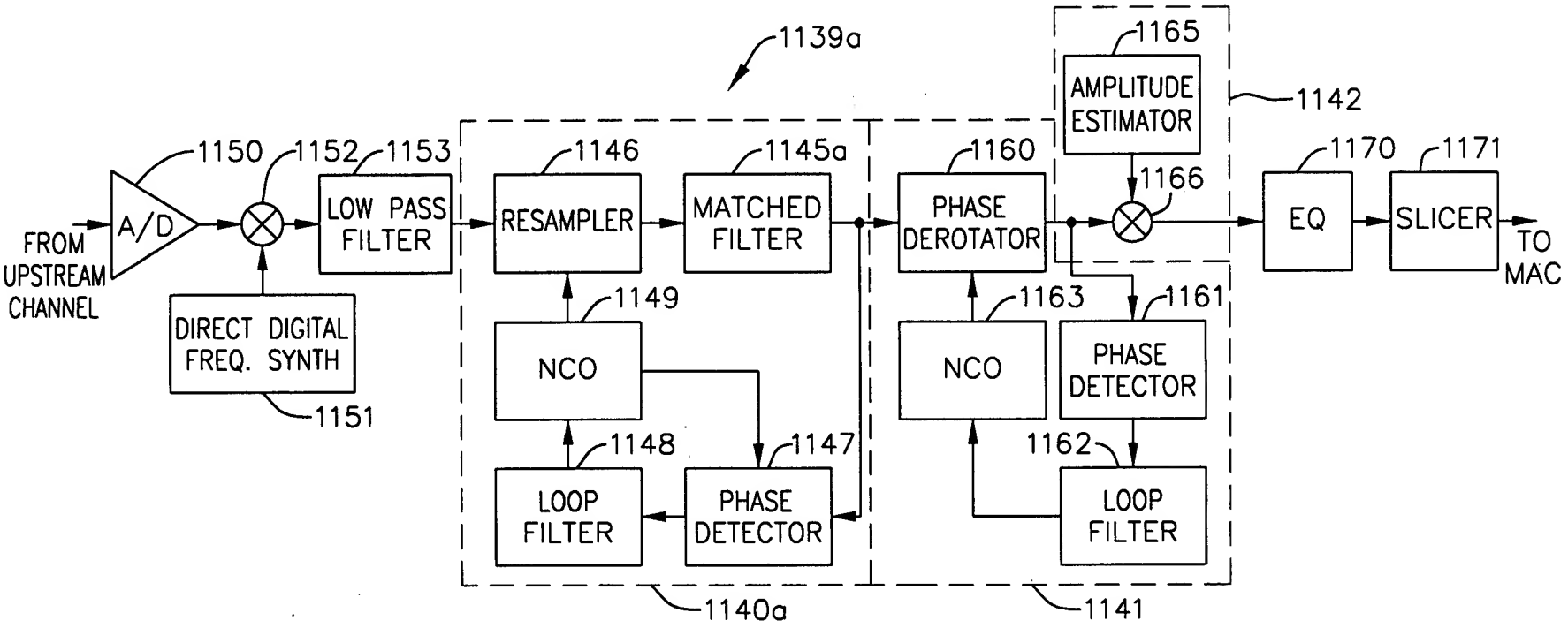

1139a
1165
AMPLITUDE ESTIMATOR
1142
1150
1152
1153
1146
1145a
1160
1170
1171
FROM UPSTREAM CHANNEL
A/D
LOW PASS FILTER
RESAMPLER
MATCHED FILTER
PHASE DEROTATOR
1166
EQ
SLICER
TO MAC
1149
1163
1161
DIRECT DIGITAL FREQ. SYNTH
NCO
NCO
PHASE DETECTOR
1151
1148
1147
1162
LOOP FILTER
PHASE DETECTOR
LOOP FILTER
1140a
1141

FIG.22

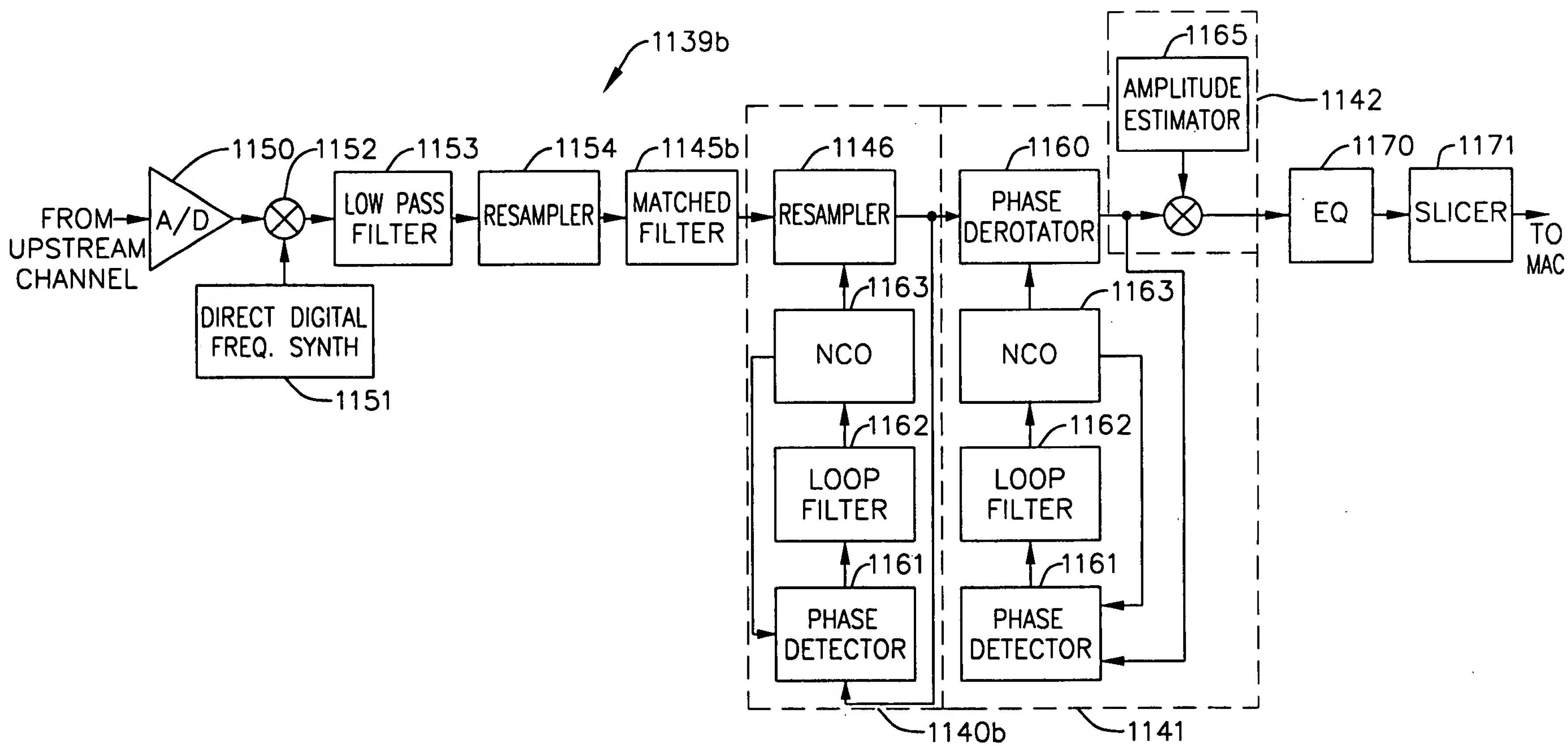

1139b
FROM UPSTREAM CHANNEL
A/D
1150
1152
1153
LOW PASS FILTER
1154
RESAMPLER
1145b
MATCHED FILTER
DIRECT DIGITAL FREQ. SYNTH
1151
1146
RESAMPLER
1163
NCO
1162
LOOP FILTER
1161
PHASE DETECTOR
1140b
1160
PHASE DEROTATOR
1163
NCO
1162
LOOP FILTER
1161
PHASE DETECTOR
1141
1165
AMPLITUDE ESTIMATOR
1142
1170
EQ
1171
SLICER
TO MAC

FIG.23

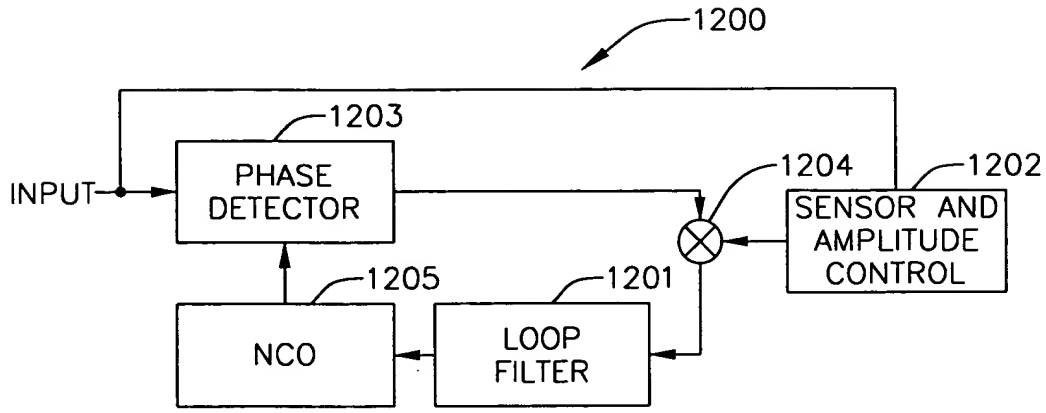

1200
1203
INPUT
PHASE DETECTOR
1204
1202
SENSOR AND AMPLITUDE CONTROL
1205
1201
NCO
LOOP FILTER

FIG.24

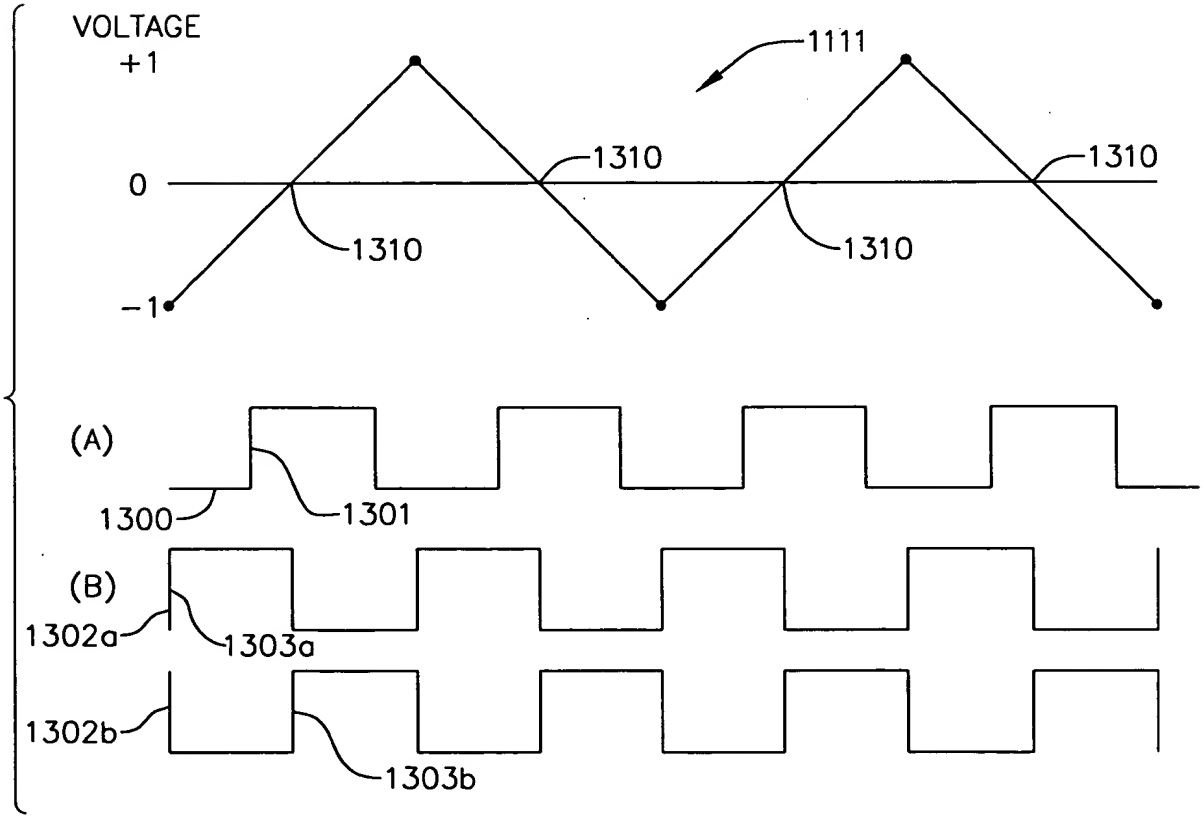

VOLTAGE
+1
0
−1
1111
1310
1310
1310
1310
(A)
1300
1301
(B)
1302a
1303a
1302b
1303b

FIG.25A

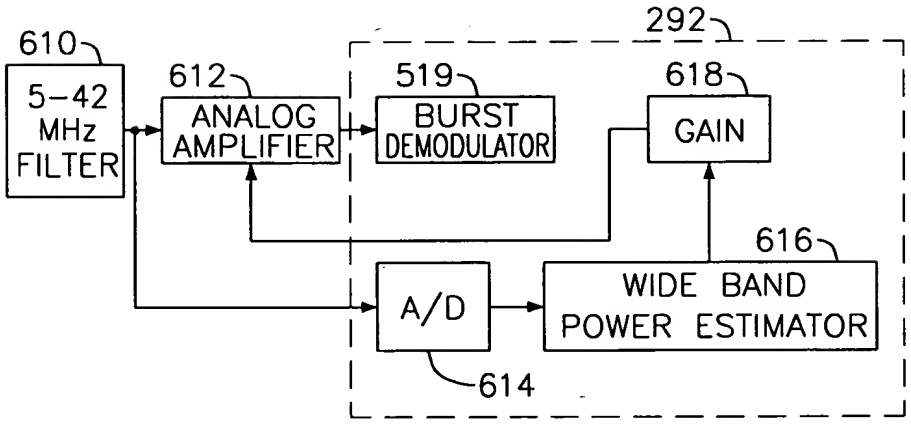


FIG.25B

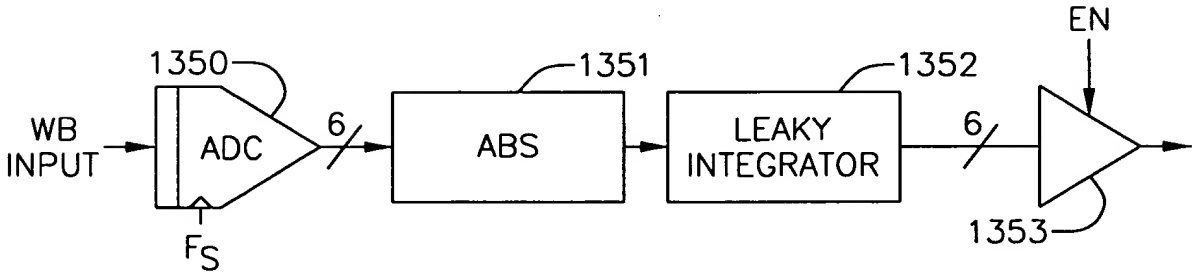


FIG.26

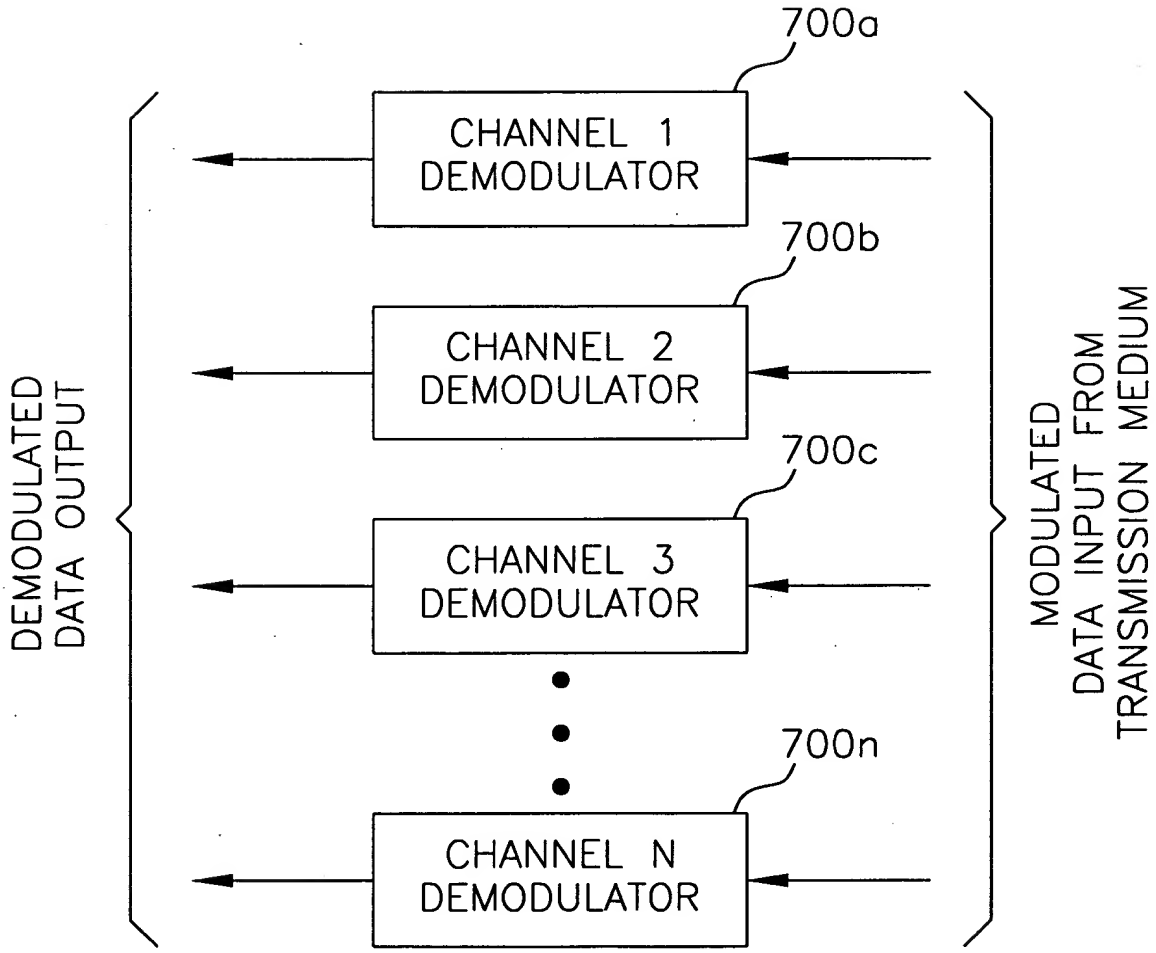

700a
CHANNEL 1 DEMODULATOR
700b
CHANNEL 2 DEMODULATOR
700c
CHANNEL 3 DEMODULATOR
700n
CHANNEL N DEMODULATOR
DEMODULATED DATA OUTPUT
MODULATED DATA INPUT FROM TRANSMISSION MEDIUM

FIG. 27

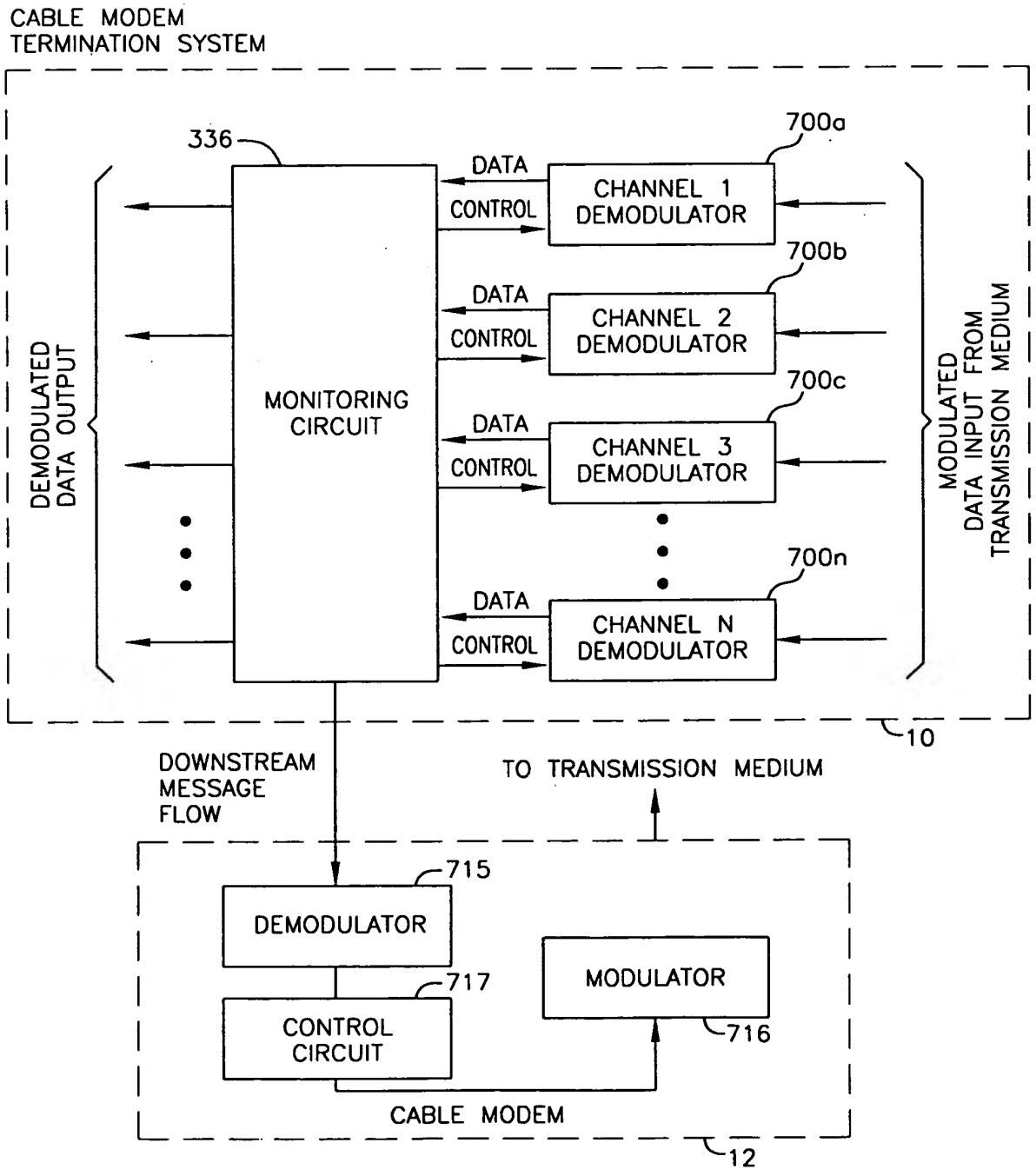

CABLE MODEM
TERMINATION SYSTEM
336
700a
700b
700c
700n
DATA
CONTROL
CHANNEL 1
DEMODULATOR
CHANNEL 2
DEMODULATOR
CHANNEL 3
DEMODULATOR
CHANNEL N
DEMODULATOR
MONITORING
CIRCUIT
DEMODULATED
DATA OUTPUT
MODULATED
DATA INPUT FROM
TRANSMISSION MEDIUM
10
DOWNSTREAM
MESSAGE
FLOW
TO TRANSMISSION MEDIUM
715
DEMODULATOR
717
CONTROL
CIRCUIT
MODULATOR
716
CABLE MODEM
12

FIG.28

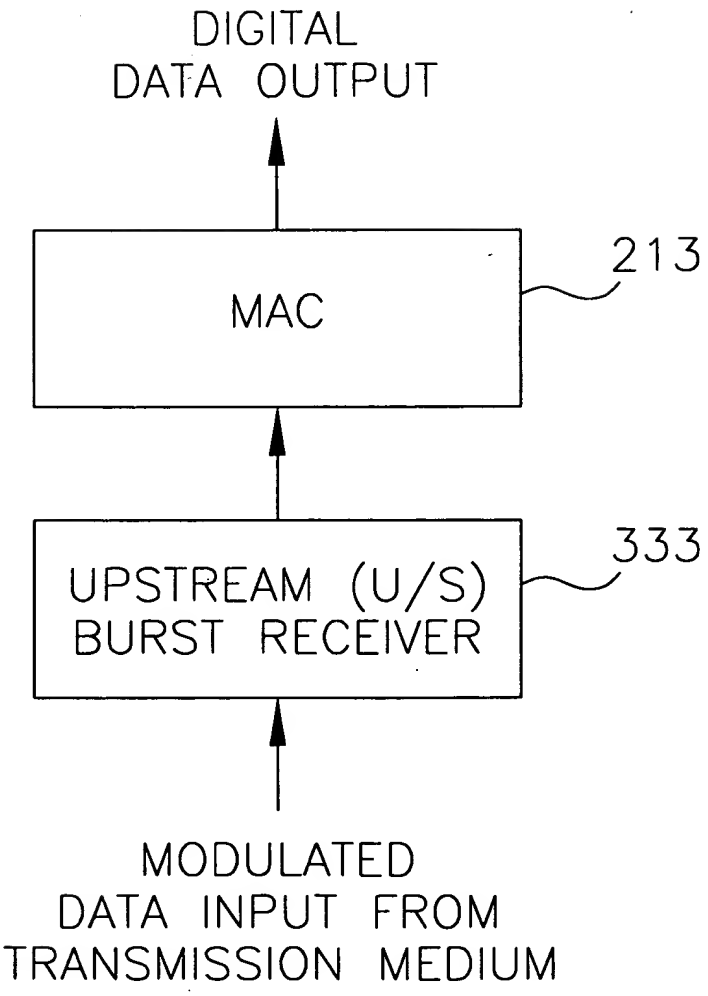

DIGITAL
DATA OUTPUT
MAC
213
UPSTREAM (U/S)
BURST RECEIVER
333
MODULATED
DATA INPUT FROM
TRANSMISSION MEDIUM

FIG.29

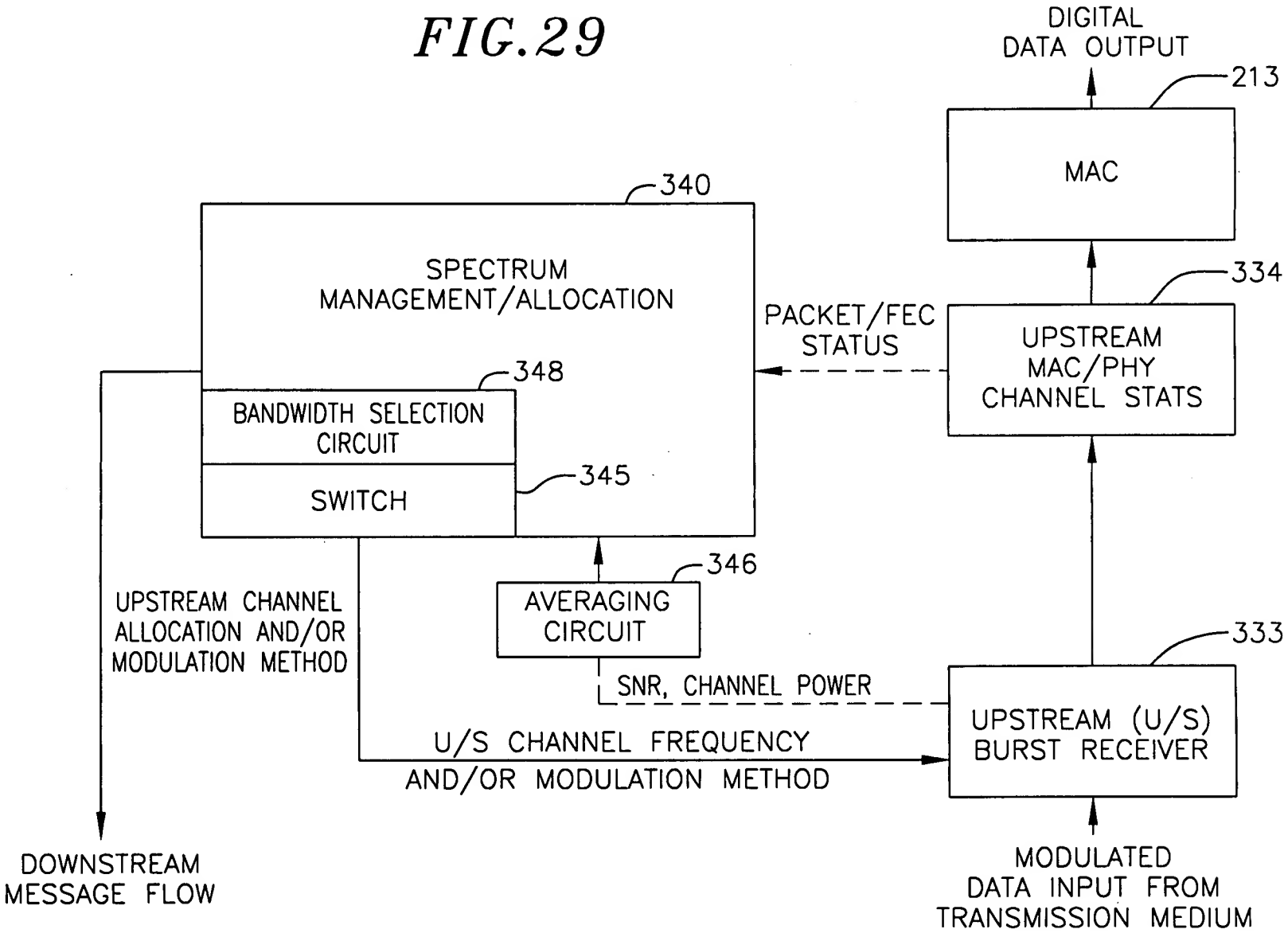

DIGITAL
DATA OUTPUT
213
MAC
340
SPECTRUM
MANAGEMENT/ALLOCATION
334
PACKET/FEC
STATUS
UPSTREAM
MAC/PHY
CHANNEL STATS
348
BANDWIDTH SELECTION
CIRCUIT
345
SWITCH
346
AVERAGING
CIRCUIT
UPSTREAM CHANNEL
ALLOCATION AND/OR
MODULATION METHOD
333
SNR, CHANNEL POWER
U/S CHANNEL FREQUENCY
AND/OR MODULATION METHOD
UPSTREAM (U/S)
BURST RECEIVER
DOWNSTREAM
MESSAGE FLOW
MODULATED
DATA INPUT FROM
TRANSMISSION MEDIUM

FIG.30

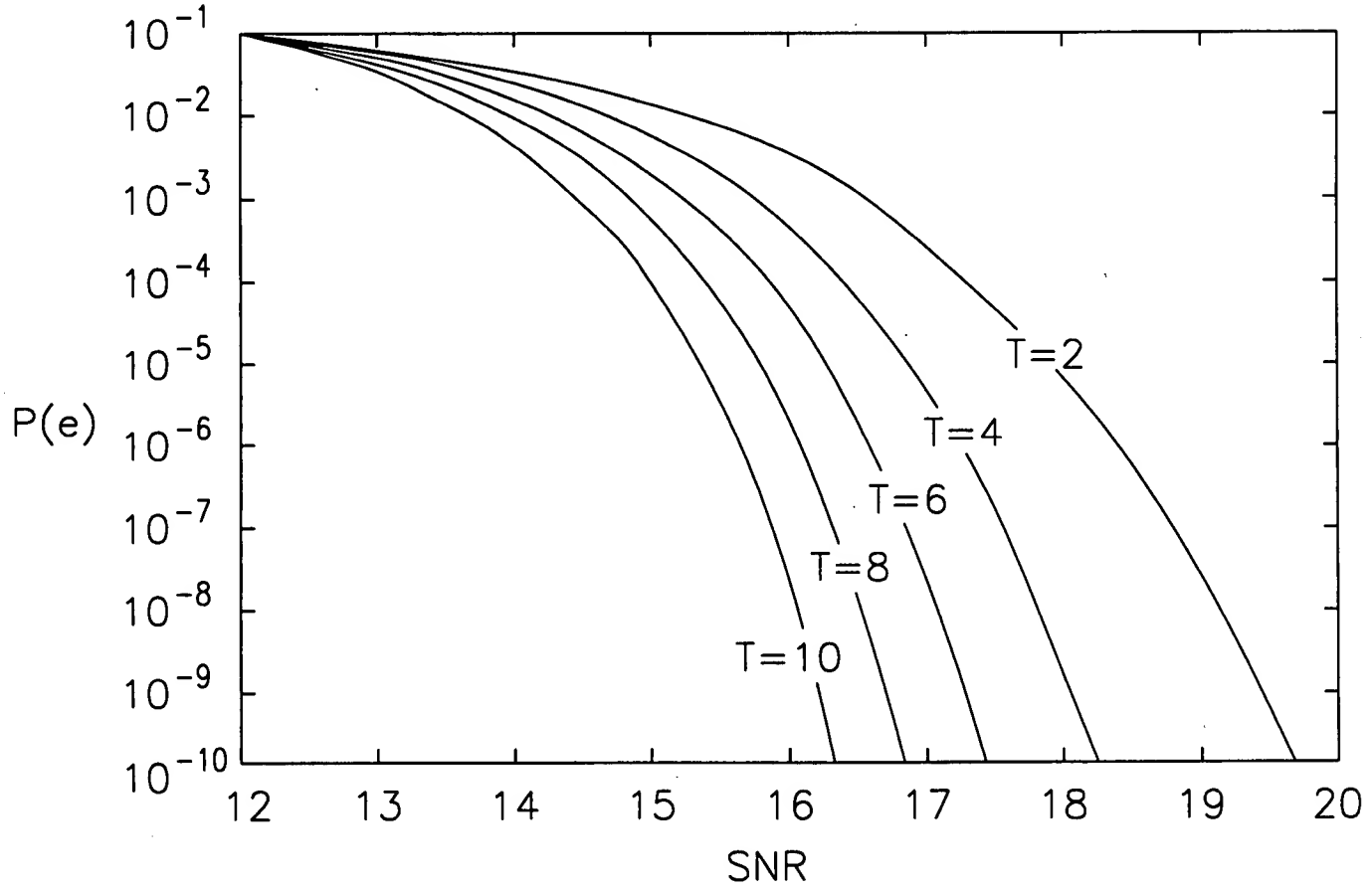

P(e)
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
12
13
14
15
16
17
18
19
20
SNR
T=2
T=4
T=6
T=8
T=10

FIG.31

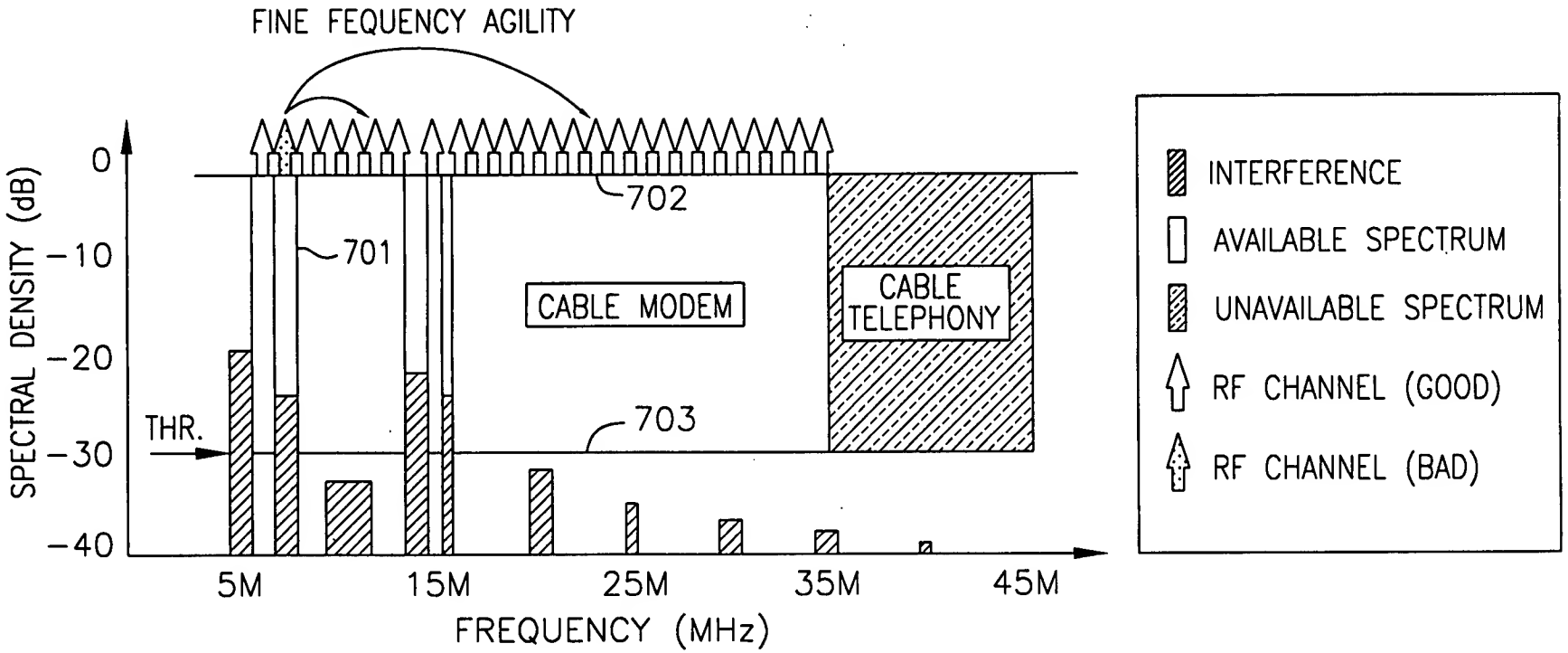

FINE FEQUENCY AGILITY
SPECTRAL DENSITY (dB)
0
-10
-20
-30
-40
THR.
701
702
703
CABLE MODEM
CABLE TELEPHONY
5M
15M
25M
35M
45M
FREQUENCY (MHz)
INTERFERENCE
AVAILABLE SPECTRUM
UNAVAILABLE SPECTRUM
RF CHANNEL (GOOD)
RF CHANNEL (BAD)

FIG.32

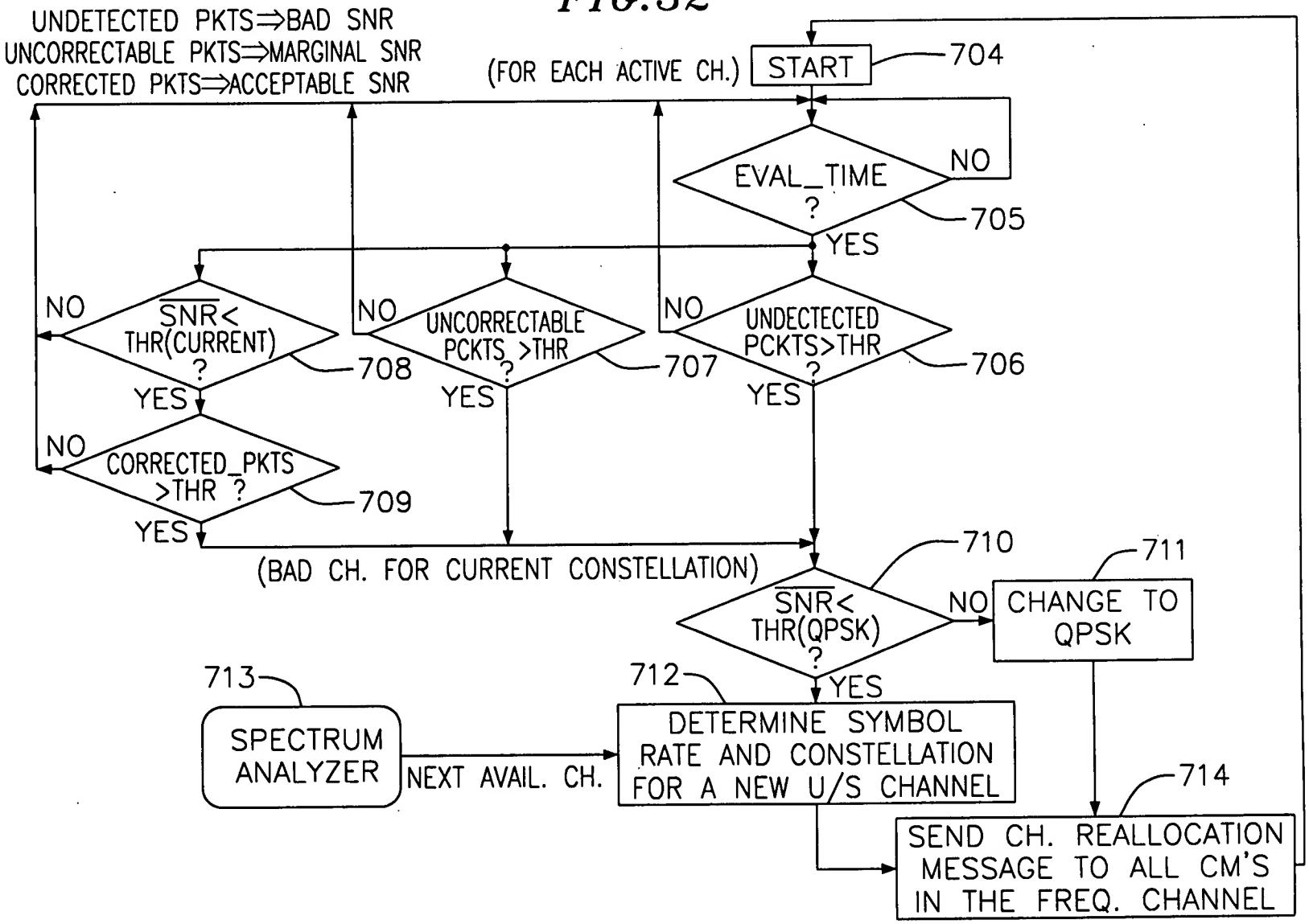

UNDETECTED PKTS⇒BAD SNR
UNCORRECTABLE PKTS⇒MARGINAL SNR
CORRECTED PKTS⇒ACCEPTABLE SNR
(FOR EACH ACTIVE CH.)
START
704
EVAL_TIME ?
NO
705
YES
NO
SNR< THR(CURRENT) ?
708
YES
NO
CORRECTED_PKTS >THR ?
709
YES
NO
UNCORRECTABLE PCKTS >THR ?
707
YES
NO
UNDECTECTED PCKTS>THR ?
706
YES
(BAD CH. FOR CURRENT CONSTELLATION)
710
SNR< THR(QPSK) ?
NO
711
CHANGE TO QPSK
YES
712
DETERMINE SYMBOL RATE AND CONSTELLATION FOR A NEW U/S CHANNEL
713
SPECTRUM ANALYZER
NEXT AVAIL. CH.
714
SEND CH. REALLOCATION MESSAGE TO ALL CM'S IN THE FREQ. CHANNEL

FIG.33

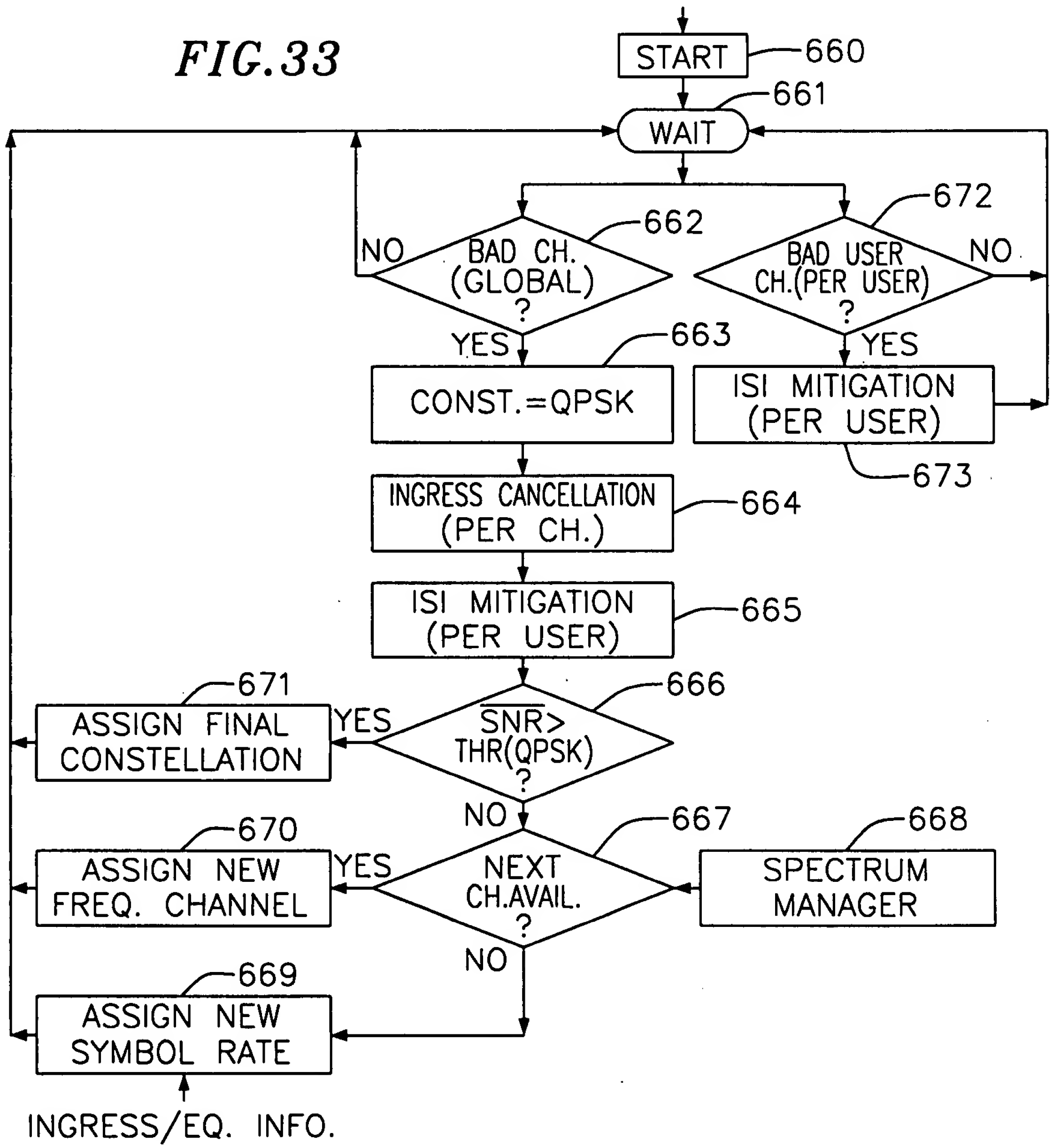


FIG.34

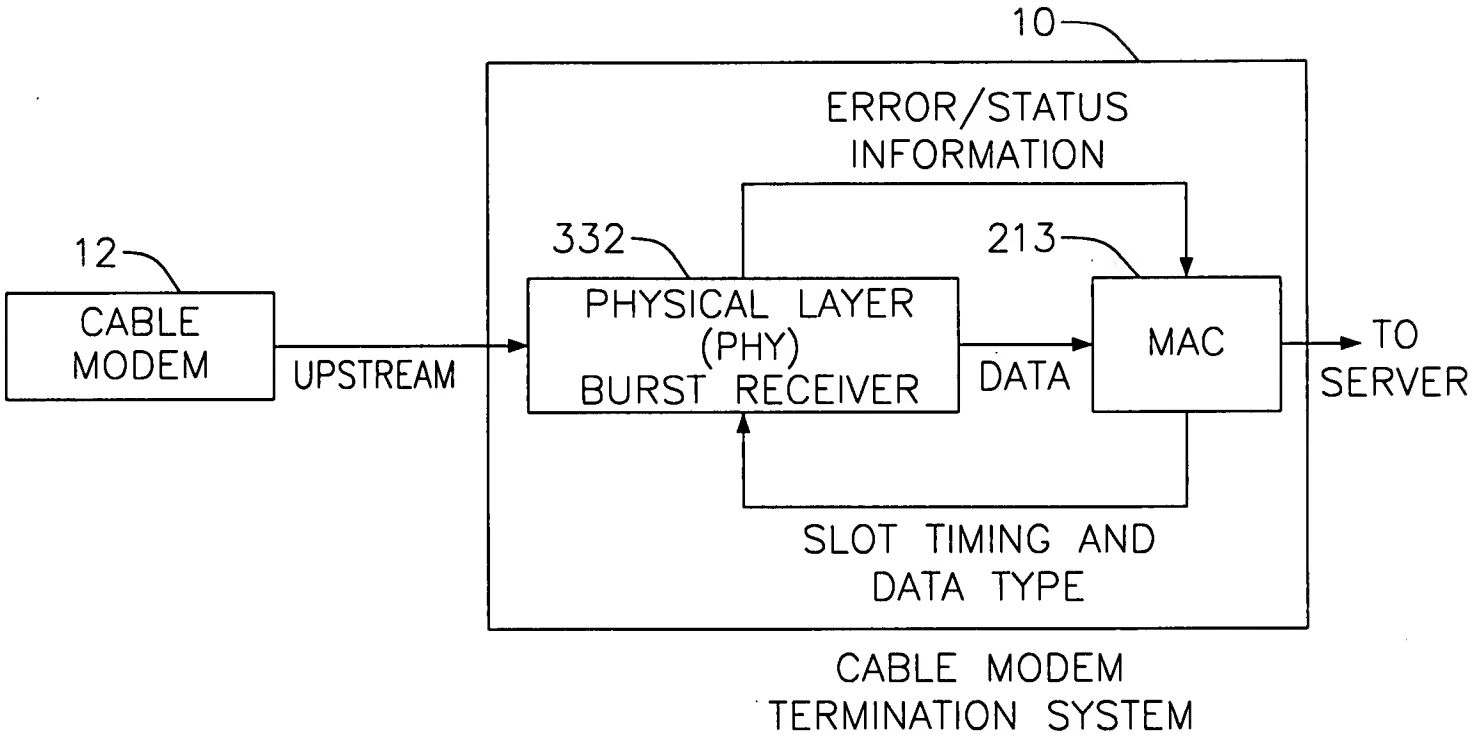

10
ERROR/STATUS
INFORMATION
12
CABLE
MODEM
UPSTREAM
332
PHYSICAL LAYER
(PHY)
BURST RECEIVER
213
MAC
DATA
TO
SERVER
SLOT TIMING AND
DATA TYPE
CABLE MODEM
TERMINATION SYSTEM

FIG.35

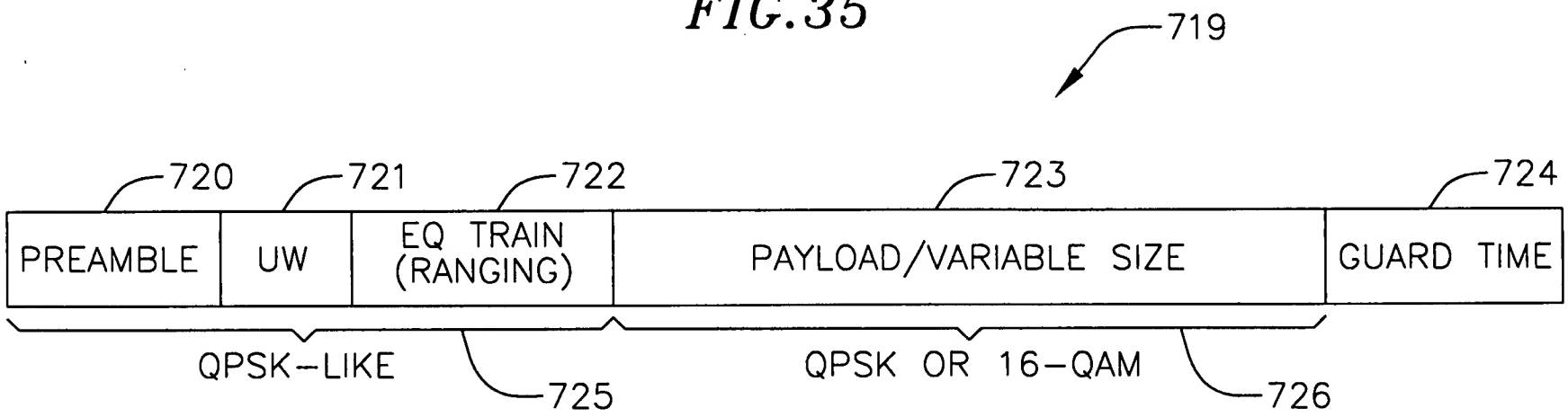

719
720
721
722
723
724
PREAMBLE
UW
EQ TRAIN (RANGING)
PAYLOAD/VARIABLE SIZE
GUARD TIME
QPSK-LIKE
QPSK OR 16-QAM
725
726

FIG.36

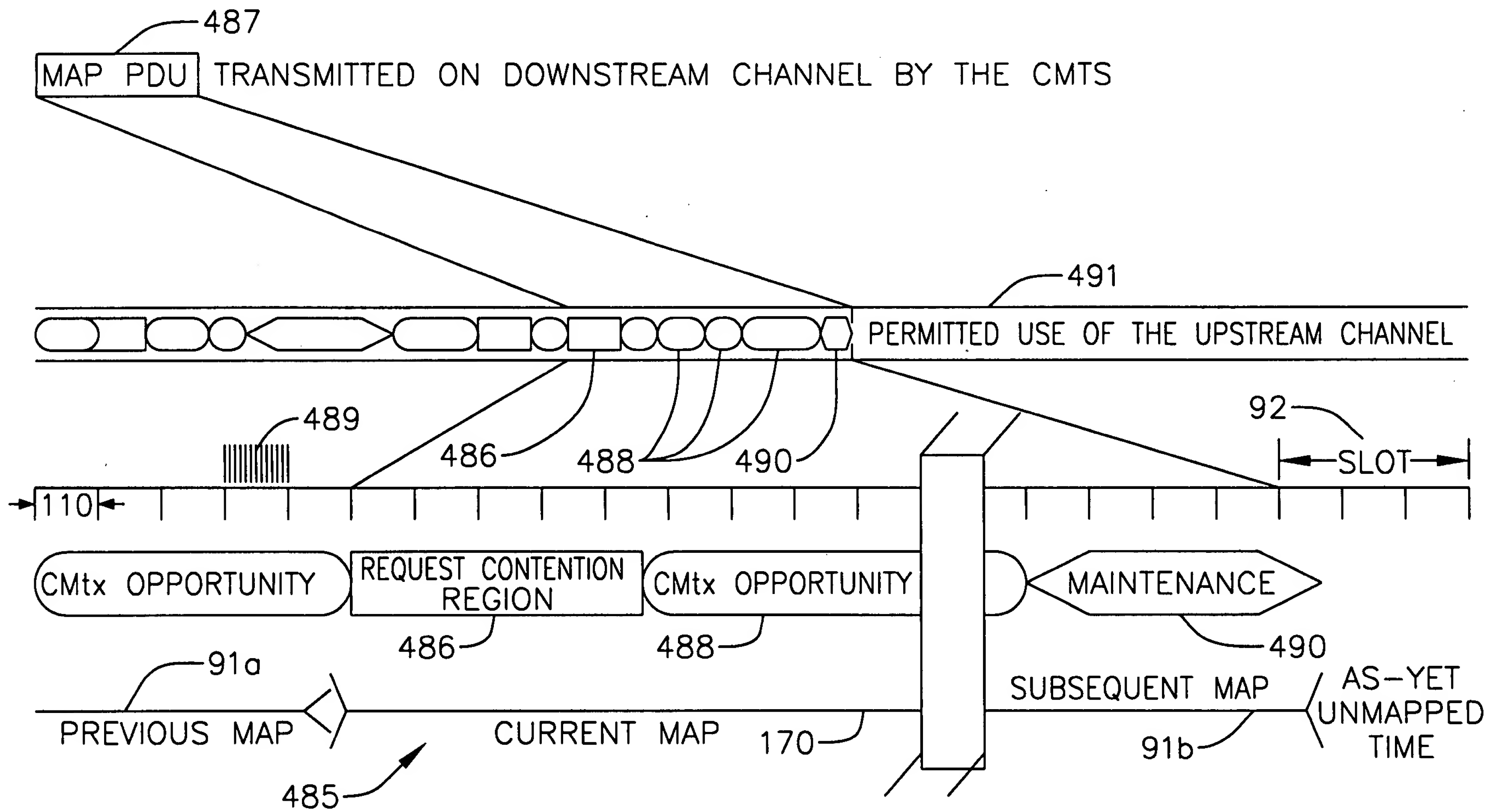

487
MAP PDU
TRANSMITTED ON DOWNSTREAM CHANNEL BY THE CMTS
491
PERMITTED USE OF THE UPSTREAM CHANNEL
489
486
488
490
92
SLOT
110
CMtx OPPORTUNITY
REQUEST CONTENTION REGION
CMtx OPPORTUNITY
MAINTENANCE
486
488
490
91a
PREVIOUS MAP
CURRENT MAP
170
SUBSEQUENT MAP
AS-YET UNMAPPED TIME
91b
485

FIG.37

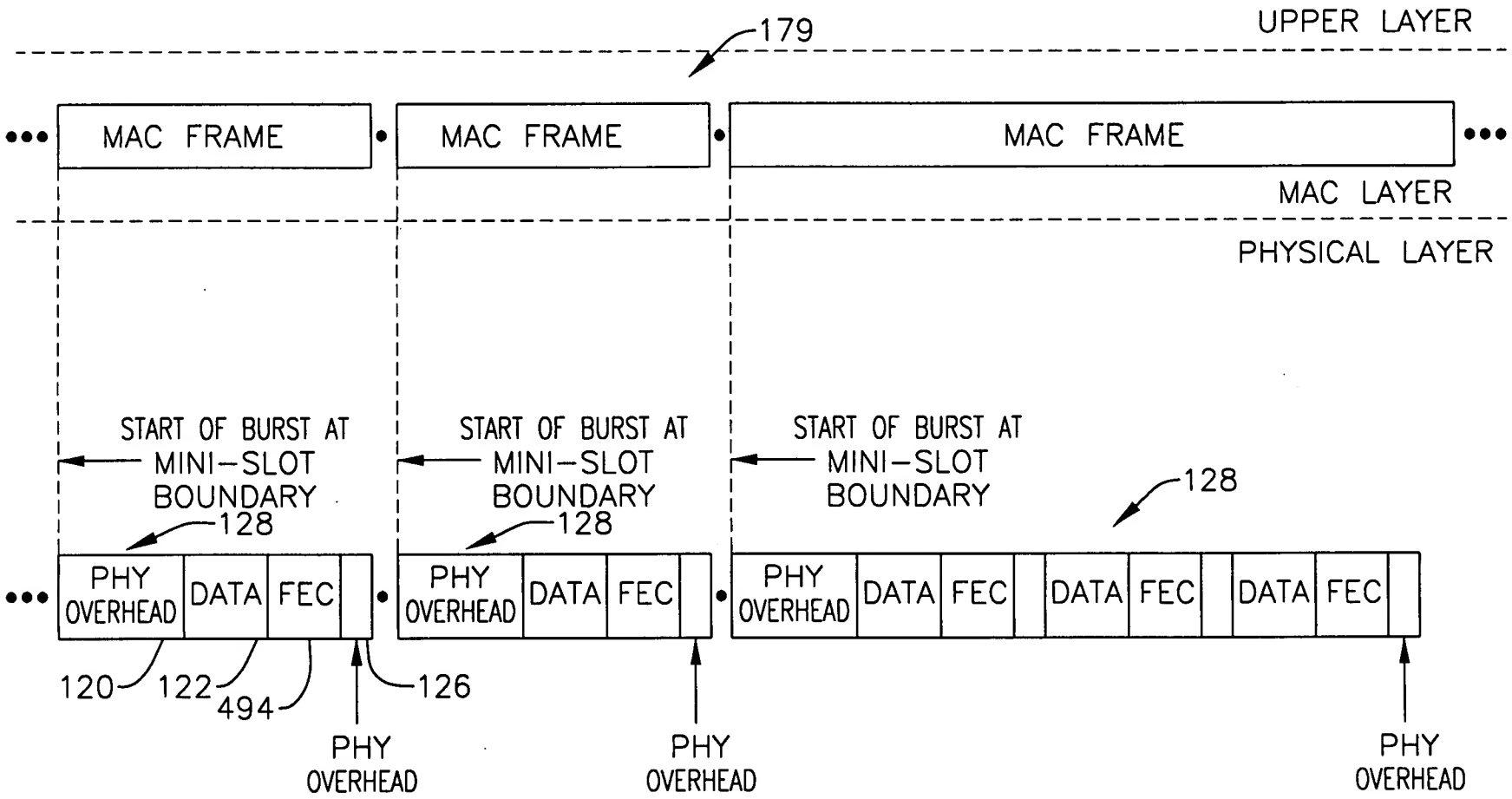
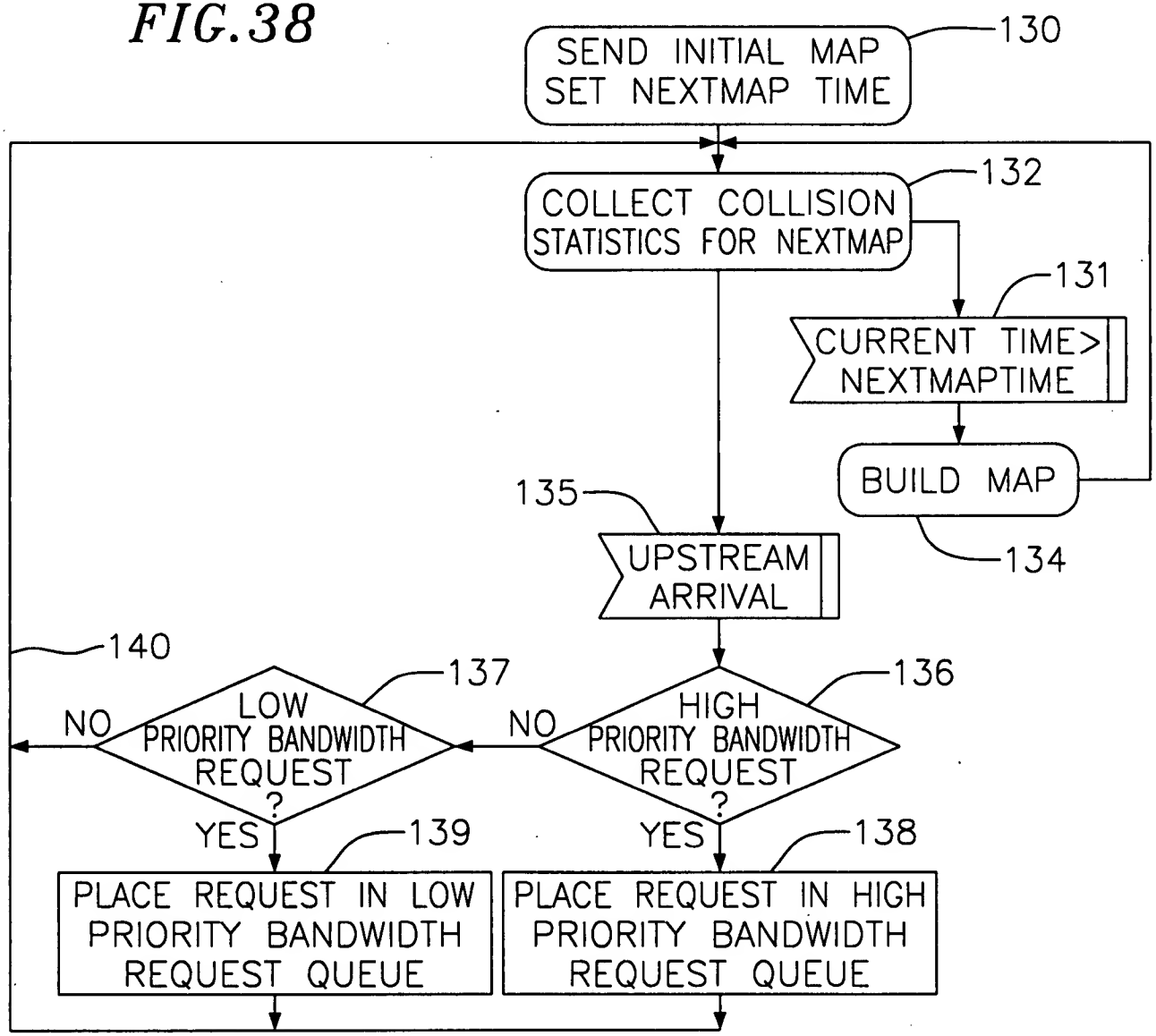

UPPER LAYER
179
MAC FRAME
MAC FRAME
MAC FRAME
MAC LAYER
PHYSICAL LAYER
START OF BURST AT MINI-SLOT BOUNDARY
128
START OF BURST AT MINI-SLOT BOUNDARY
128
START OF BURST AT MINI-SLOT BOUNDARY
128
PHY OVERHEAD
DATA
FEC
120
122
494
126
PHY OVERHEAD
PHY OVERHEAD
PHY OVERHEAD

FIG.38


SEND INITIAL MAP
SET NEXTMAP TIME
130
COLLECT COLLISION
STATISTICS FOR NEXTMAP
132
131
CURRENT TIME>
NEXTMAPTIME
BUILD MAP
134
135
UPSTREAM
ARRIVAL
140
137
136
NO
LOW
PRIORITY BANDWIDTH
REQUEST
?
NO
HIGH
PRIORITY BANDWIDTH
REQUEST
?
YES
YES
139
138
PLACE REQUEST IN LOW
PRIORITY BANDWIDTH
REQUEST QUEUE
PLACE REQUEST IN HIGH
PRIORITY BANDWIDTH
REQUEST QUEUE

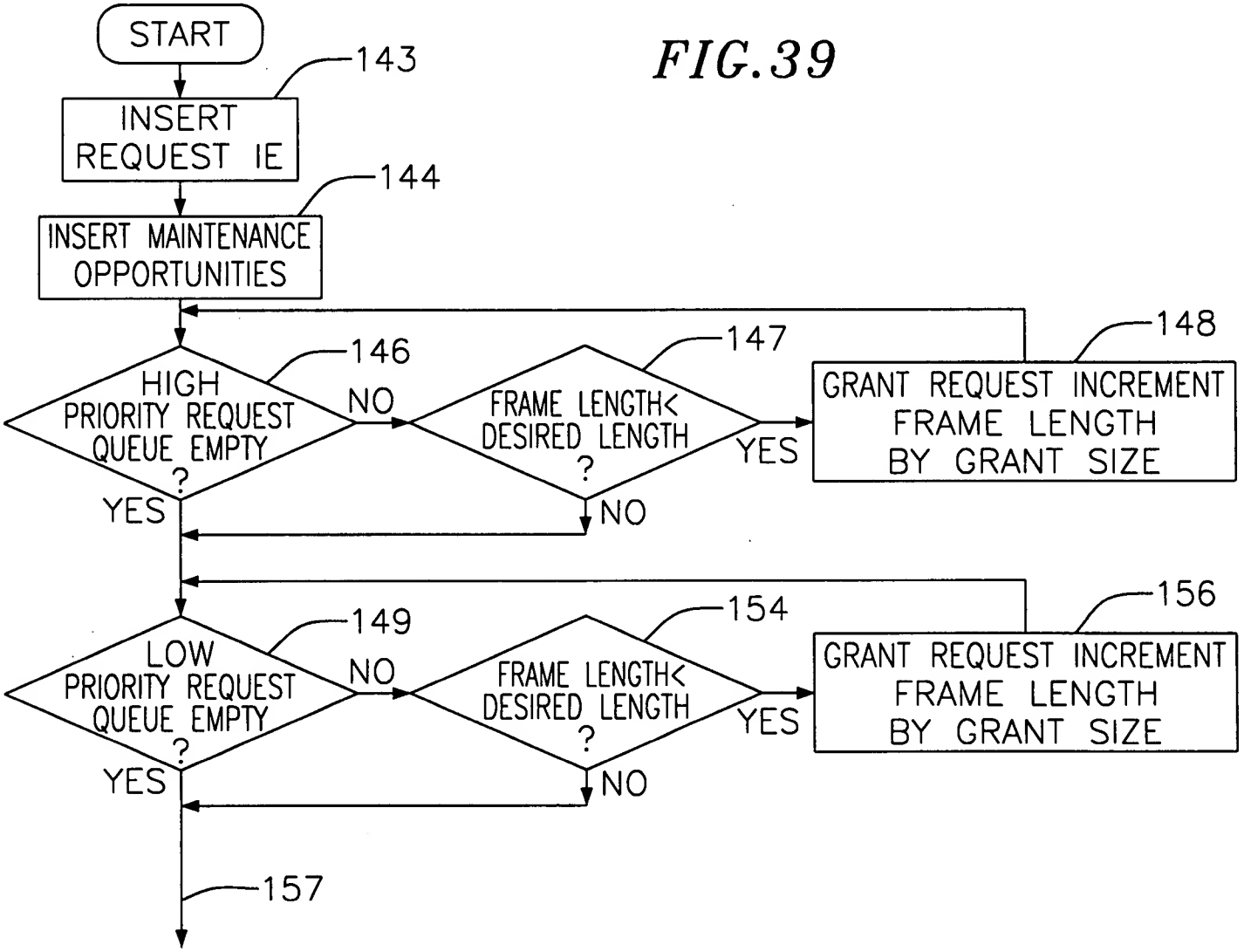

START
143
INSERT REQUEST IE
144
INSERT MAINTENANCE OPPORTUNITIES
146
HIGH PRIORITY REQUEST QUEUE EMPTY ?
NO
147
FRAME LENGTH< DESIRED LENGTH ?
YES
148
GRANT REQUEST INCREMENT FRAME LENGTH BY GRANT SIZE
YES
NO
149
LOW PRIORITY REQUEST QUEUE EMPTY ?
NO
154
FRAME LENGTH< DESIRED LENGTH ?
YES
156
GRANT REQUEST INCREMENT FRAME LENGTH BY GRANT SIZE
YES
NO
157

FIG.39

FIG.40

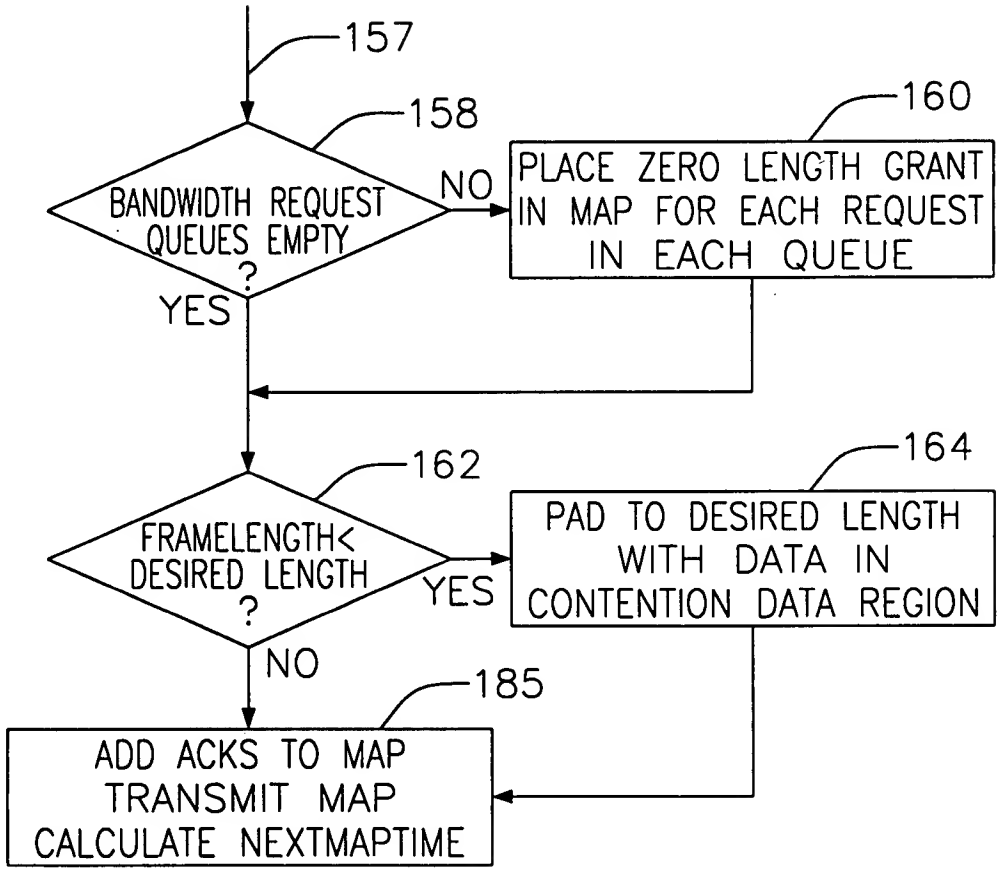

157
158
BANDWIDTH REQUEST QUEUES EMPTY ?
NO
YES
160
PLACE ZERO LENGTH GRANT IN MAP FOR EACH REQUEST IN EACH QUEUE
162
FRAMELENGTH< DESIRED LENGTH ?
YES
NO
164
PAD TO DESIRED LENGTH WITH DATA IN CONTENTION DATA REGION
185
ADD ACKS TO MAP
TRANSMIT MAP
CALCULATE NEXTMAPTIME

FIG. 41

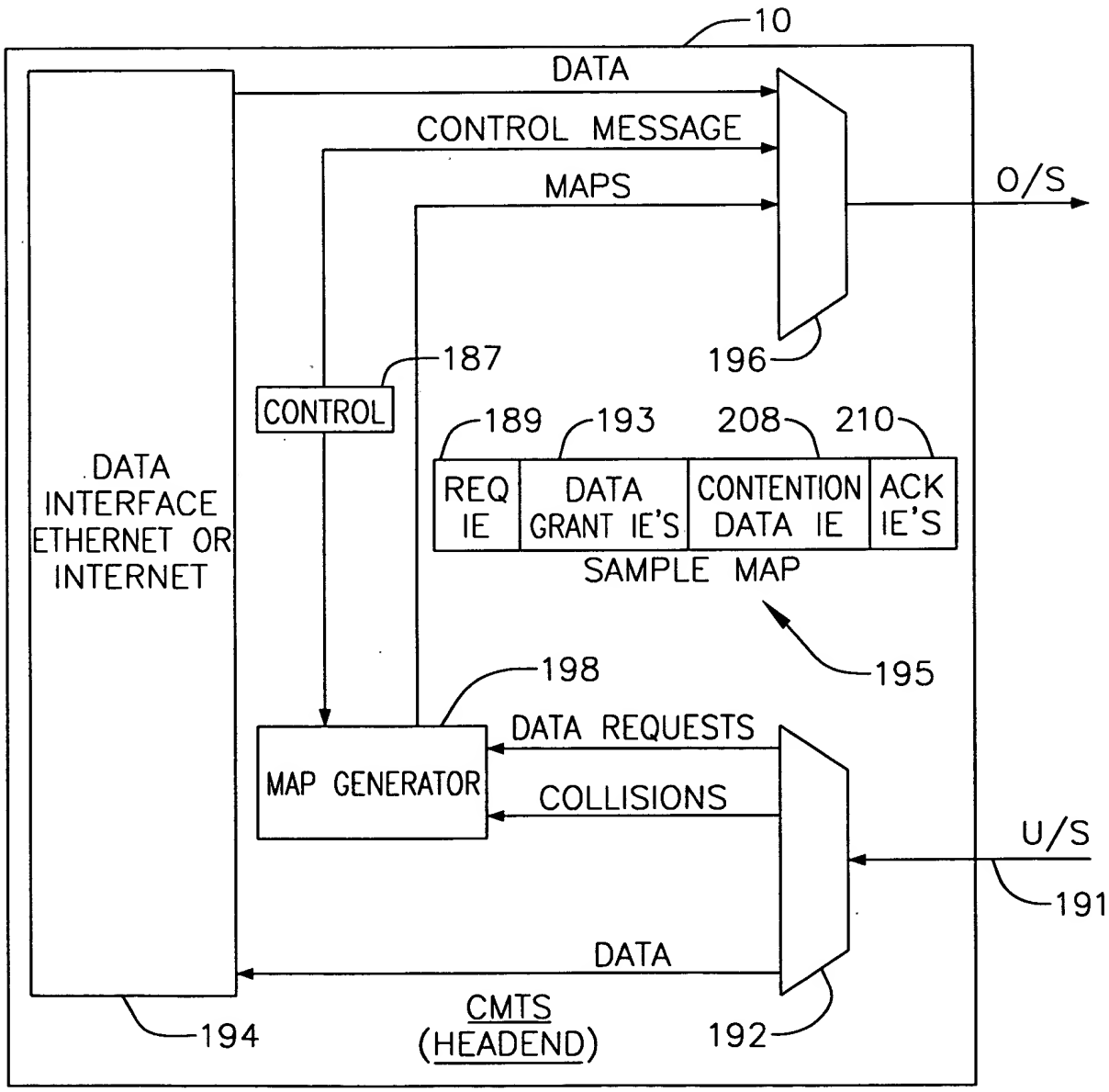

10
DATA
CONTROL MESSAGE
MAPS
O/S
196
187
CONTROL
189
193
208
210
REQ IE
DATA GRANT IE'S
CONTENTION DATA IE
ACK IE'S
SAMPLE MAP
195
DATA INTERFACE ETHERNET OR INTERNET
198
DATA REQUESTS
MAP GENERATOR
COLLISIONS
U/S
191
DATA
CMTS (HEADEND)
194
192

FIG. 42

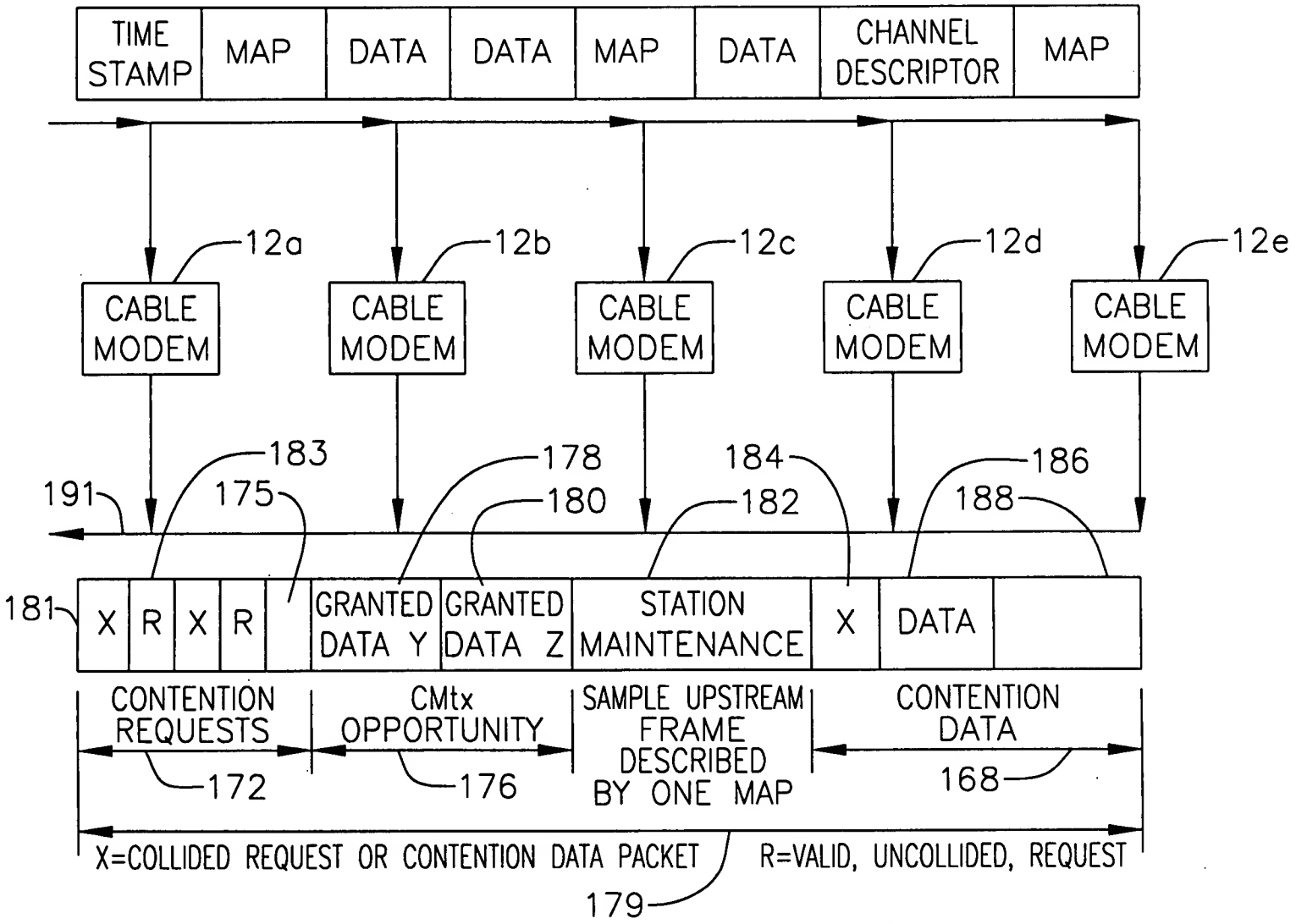
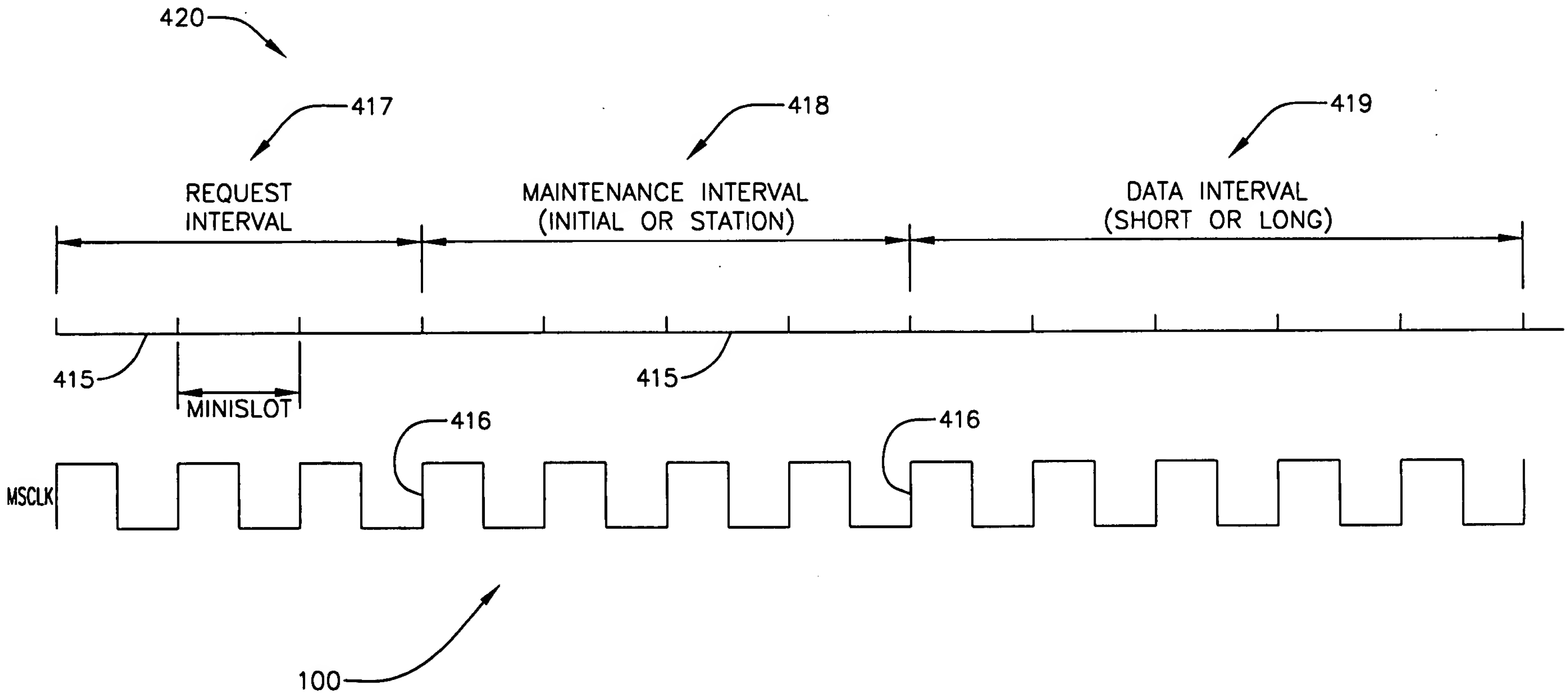

TIME STAMP
MAP
DATA
DATA
MAP
DATA
CHANNEL DESCRIPTOR
MAP
12a
12b
12c
12d
12e
CABLE MODEM
CABLE MODEM
CABLE MODEM
CABLE MODEM
CABLE MODEM
191
183
175
178
180
184
182
186
188
181
X
R
X
R
GRANTED DATA Y
GRANTED DATA Z
STATION MAINTENANCE
X
DATA
CONTENTION REQUESTS
CMtx OPPORTUNITY
SAMPLE UPSTREAM FRAME DESCRIBED BY ONE MAP
CONTENTION DATA
172
176
168
X=COLLIDED REQUEST OR CONTENTION DATA PACKET
R=VALID, UNCOLLIDED, REQUEST
179

FIG. 43



420
417
418
419
REQUEST INTERVAL
MAINTENANCE INTERVAL (INITIAL OR STATION)
DATA INTERVAL (SHORT OR LONG)
415
MINISLOT
415
416
416
MSCLK
100

FIG.44

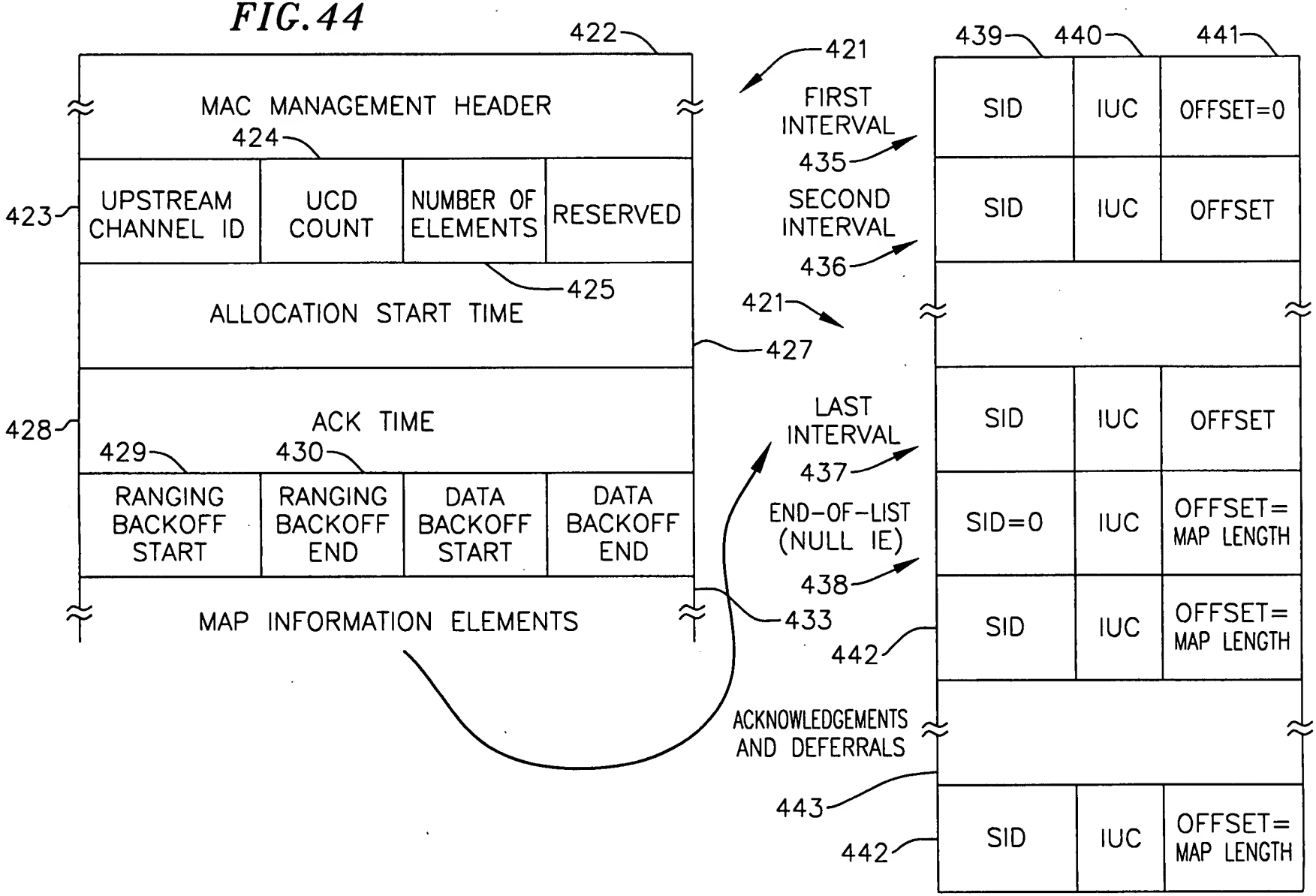

422
421
439
440
441
MAC MANAGEMENT HEADER
424
FIRST INTERVAL
435
SID
IUC
OFFSET=0
423
UPSTREAM CHANNEL ID
UCD COUNT
NUMBER OF ELEMENTS
RESERVED
SECOND INTERVAL
436
SID
IUC
OFFSET
425
ALLOCATION START TIME
421
427
428
ACK TIME
LAST INTERVAL
437
SID
IUC
OFFSET
429
430
RANGING BACKOFF START
RANGING BACKOFF END
DATA BACKOFF START
DATA BACKOFF END
END-OF-LIST (NULL IE)
438
SID=0
IUC
OFFSET= MAP LENGTH
MAP INFORMATION ELEMENTS
433
442
SID
IUC
OFFSET= MAP LENGTH
ACKNOWLEDGEMENTS AND DEFERRALS
443
442
SID
IUC
OFFSET= MAP LENGTH

FIG.45

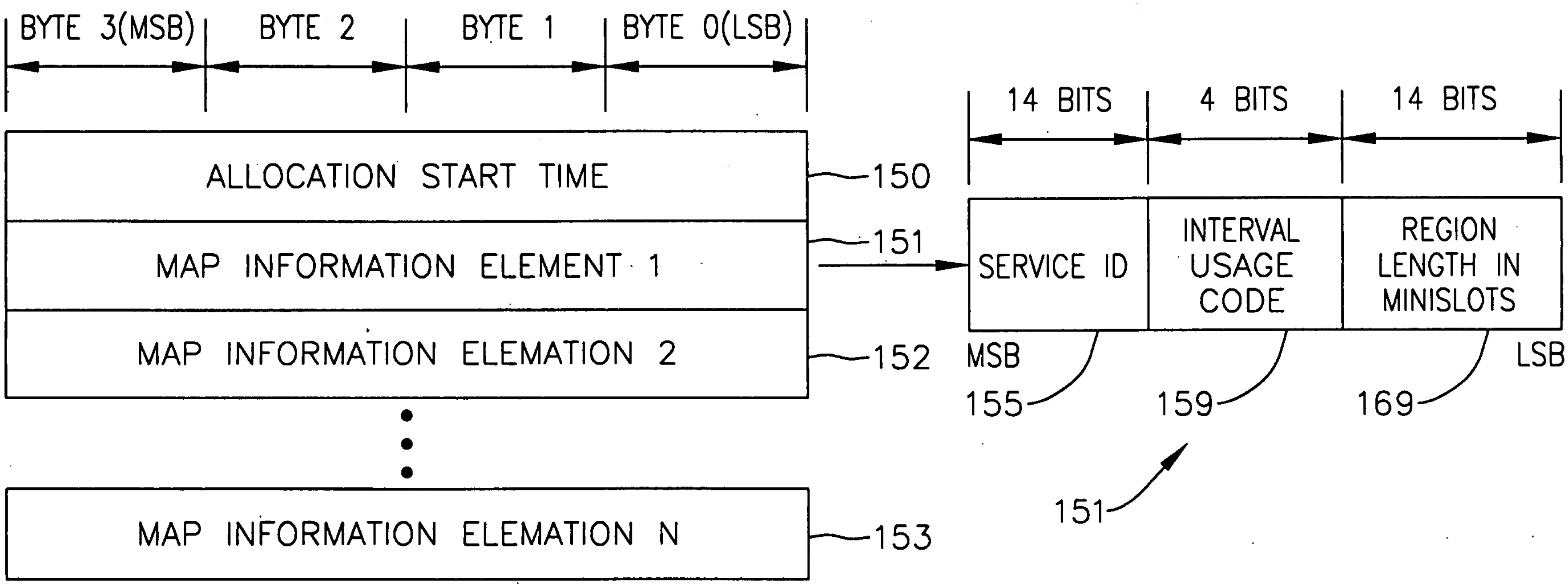

BYTE 3(MSB)
BYTE 2
BYTE 1
BYTE 0(LSB)
ALLOCATION START TIME
MAP INFORMATION ELEMENT 1
MAP INFORMATION ELEMATION 2
MAP INFORMATION ELEMATION N
150
151
152
153
14 BITS
4 BITS
14 BITS
SERVICE ID
INTERVAL USAGE CODE
REGION LENGTH IN MINISLOTS
MSB
LSB
155
159
169
151

FIG.46

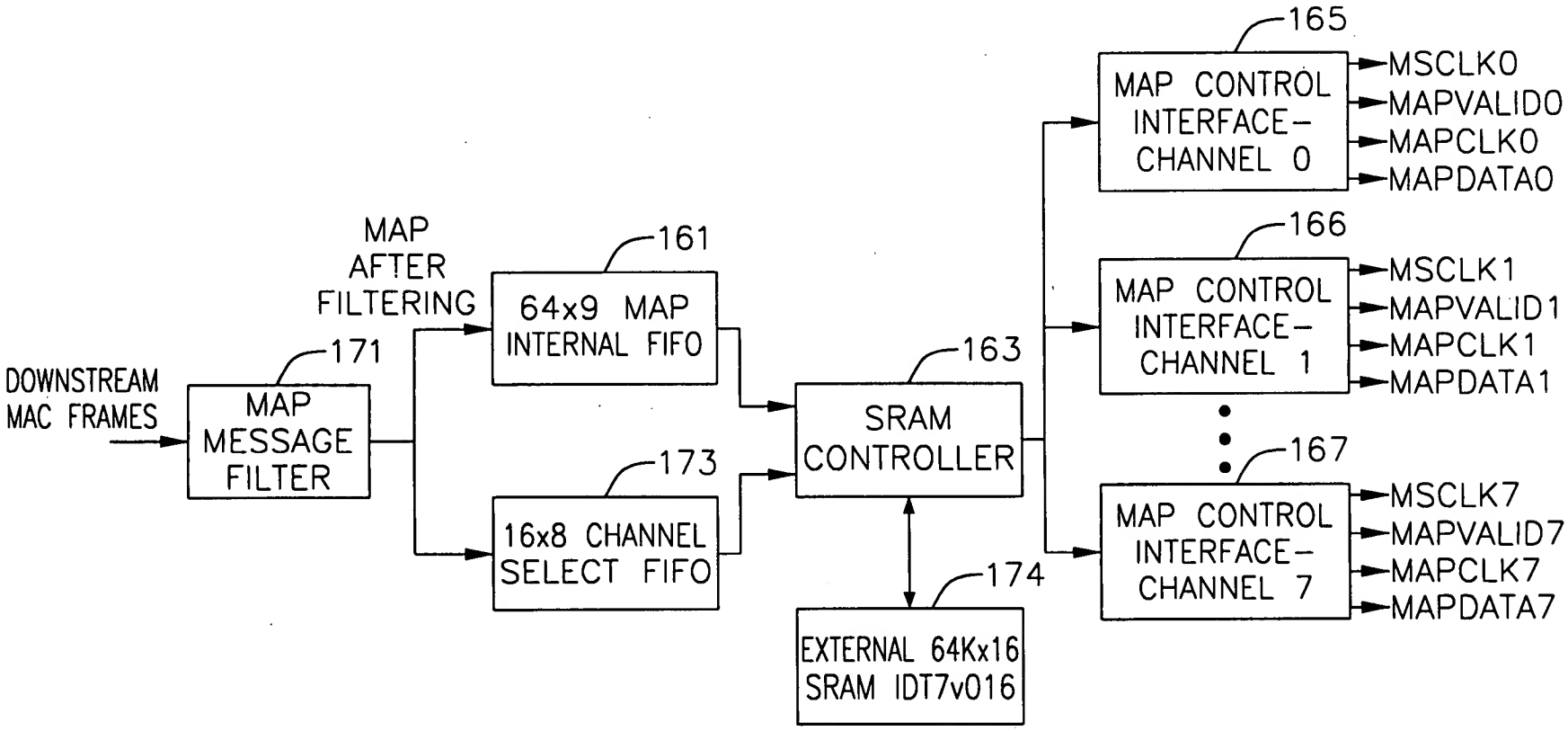

DOWNSTREAM MAC FRAMES
MAP MESSAGE FILTER
171
MAP AFTER FILTERING
64x9 MAP INTERNAL FIFO
161
16x8 CHANNEL SELECT FIFO
173
SRAM CONTROLLER
163
EXTERNAL 64Kx16 SRAM IDT7v016
174
MAP CONTROL INTERFACE- CHANNEL 0
165
MSCLK0
MAPVALIDO
MAPCLK0
MAPDATAO
MAP CONTROL INTERFACE- CHANNEL 1
166
MSCLK1
MAPVALID1
MAPCLK1
MAPDATA1
MAP CONTROL INTERFACE- CHANNEL 7
167
MSCLK7
MAPVALID7
MAPCLK7
MAPDATA7

FIG. 47

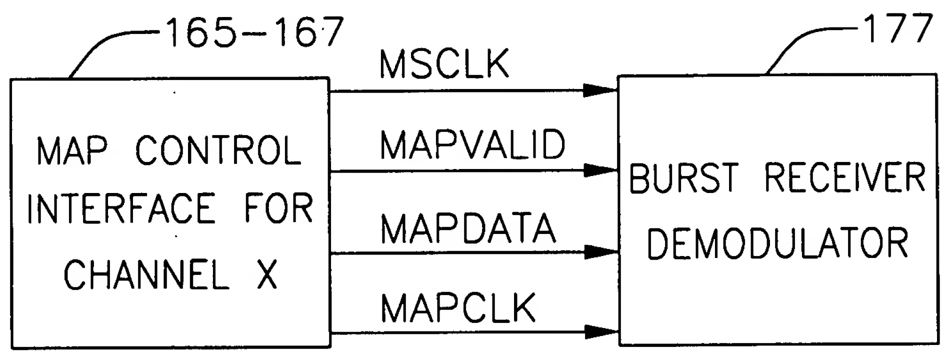

165-167
MAP CONTROL INTERFACE FOR CHANNEL X
MSCLK
MAPVALID
MAPDATA
MAPCLK
177
BURST RECEIVER DEMODULATOR

FIG. 48

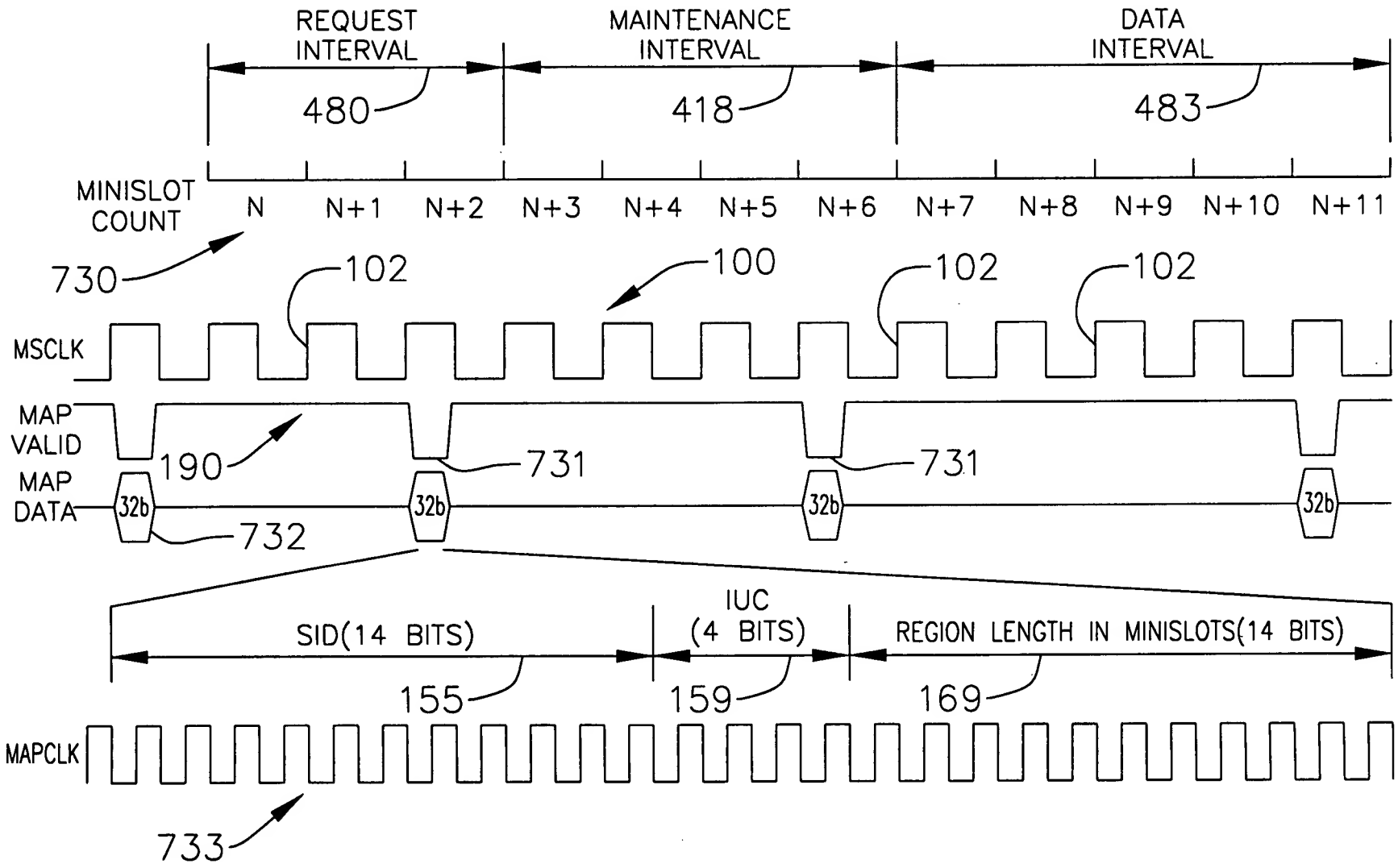
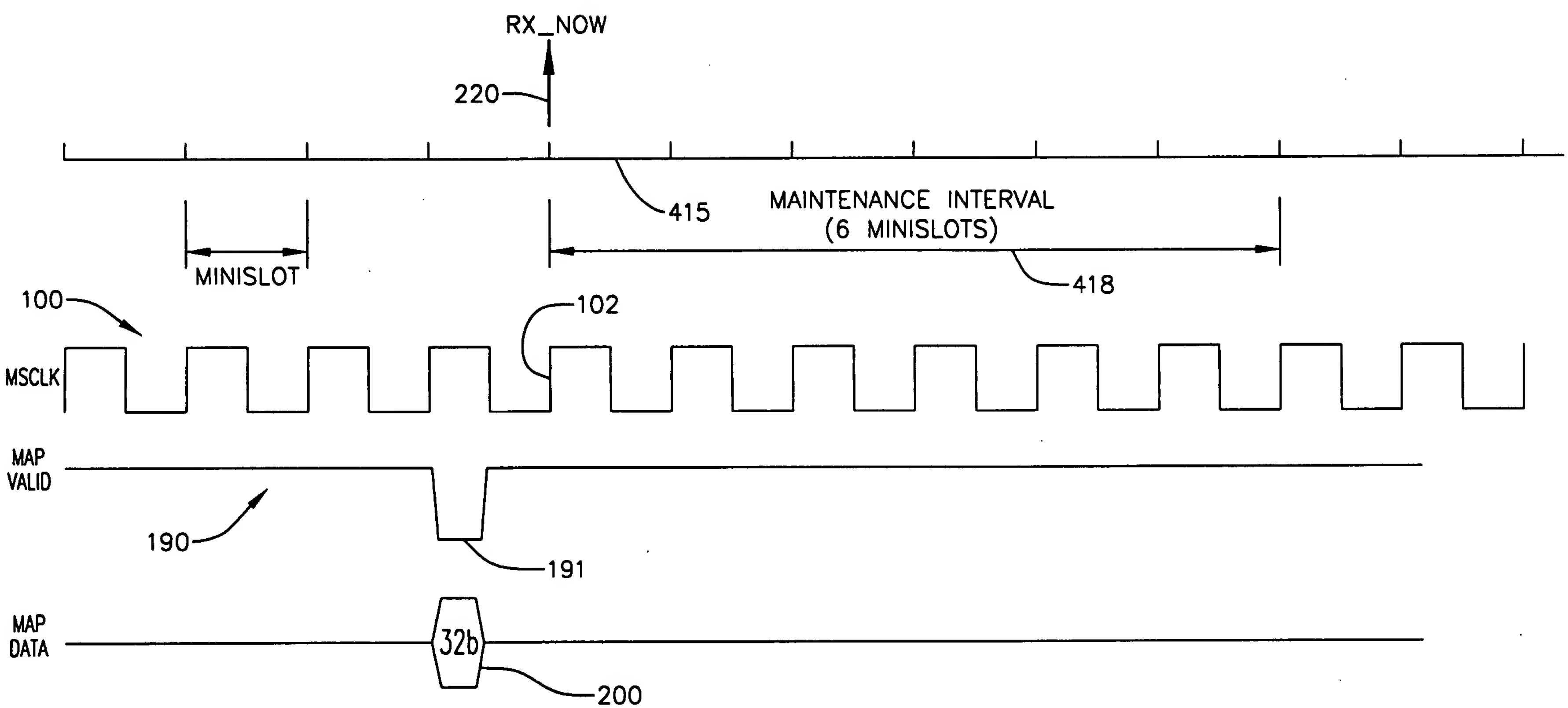

REQUEST INTERVAL
MAINTENANCE INTERVAL
DATA INTERVAL
480
418
483
MINISLOT COUNT
N
N+1
N+2
N+3
N+4
N+5
N+6
N+7
N+8
N+9
N+10
N+11
730
102
100
102
102
MSCLK
MAP VALID
190
731
731
MAP DATA
32b
32b
32b
32b
732
SID(14 BITS)
IUC (4 BITS)
REGION LENGTH IN MINISLOTS(14 BITS)
155
159
169
MAPCLK
733

FIG.49



RX_NOW
220
415
MAINTENANCE INTERVAL
(6 MINISLOTS)
418
MINISLOT
100
102
MSCLK
MAP
VALID
190
191
MAP
DATA
32b
200

FIG.50

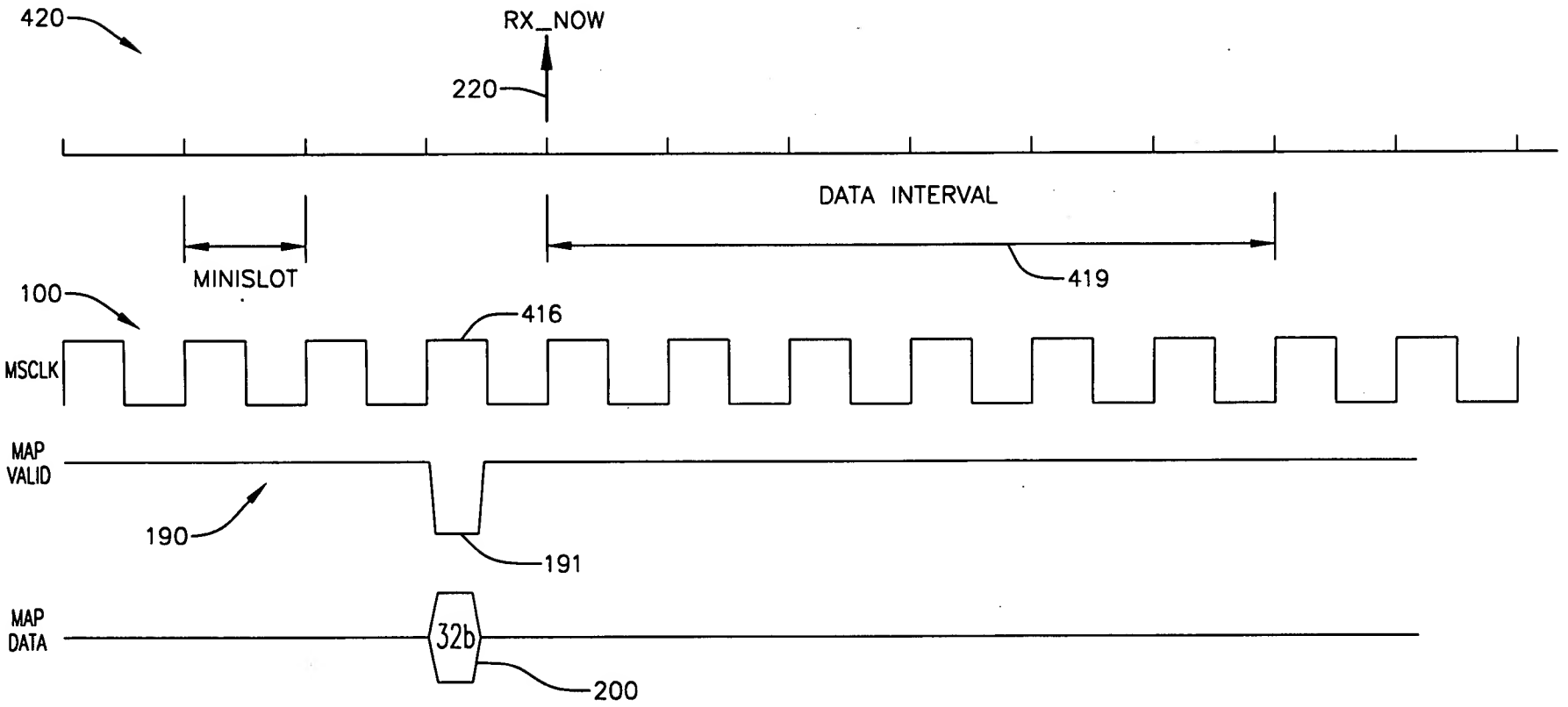

420
RX_NOW
220
DATA INTERVAL
MINISLOT
419
100
416
MSCLK
MAP VALID
190
191
MAP DATA
32b
200

FIG.51

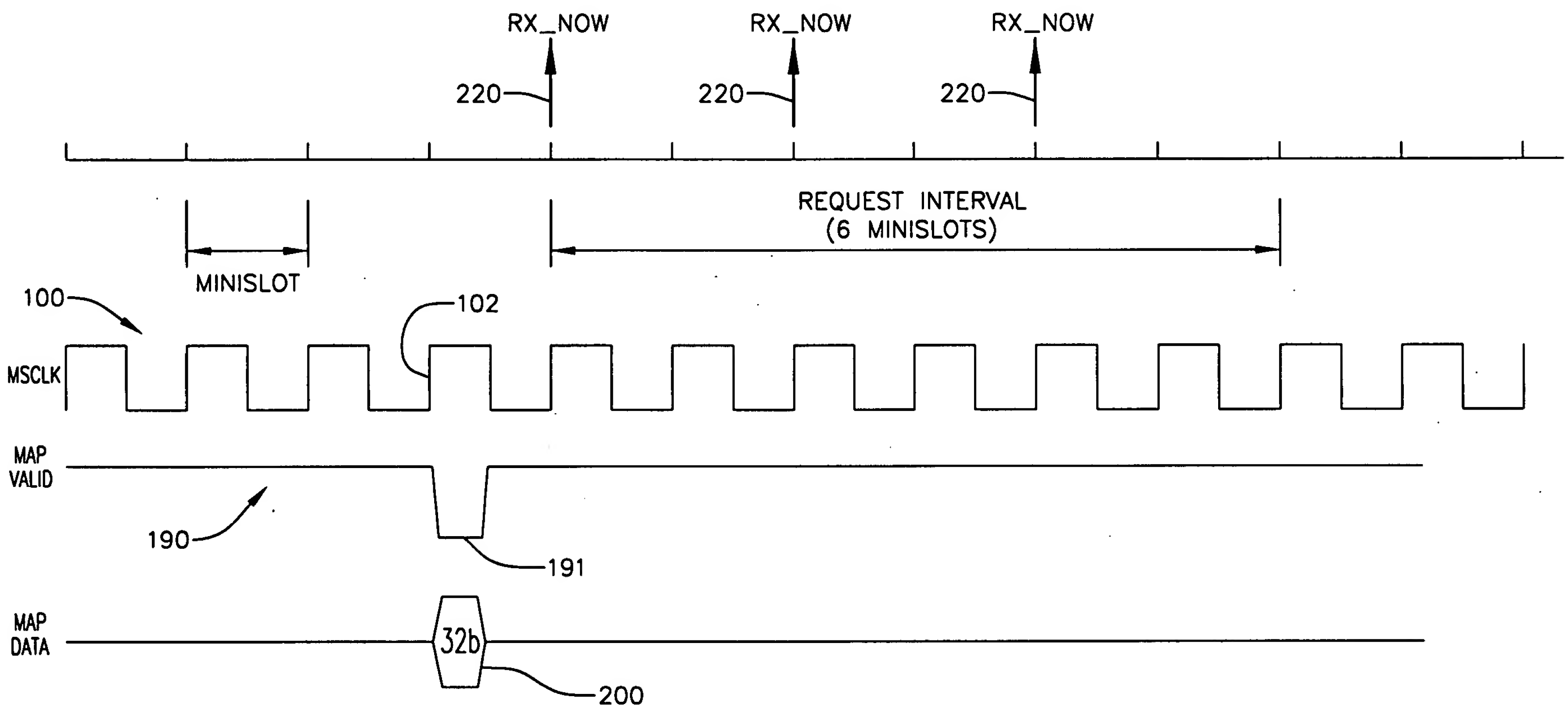

RX_NOW
RX_NOW
RX_NOW
220
220
220
REQUEST INTERVAL
(6 MINISLOTS)
MINISLOT
100
102
MSCLK
MAP
VALID
190
191
MAP
DATA
32b
200

FIG.52

RNG. OFFSET 7 BYTES

STATUS 2 BYTES	TIMESTAMP 4 BYTES	CH. ID 1 BYTE	SID 2 BYTES	PWR. 2 BYTES	FREQ. 2 BYTES	TIME 3 BYTES

FIG.53

RNG. OFFSET 7 BYTES

STATUS 2 BYTES	TIMESTAMP 4 BYTES	CH. ID 1 BYTE	SID 2 BYTES	PWR. 2 BYTES	FREQ. 2 BYTES	TIME 3 BYTES	EQUALIZER COEFFS. 32 BYTES

FIG.54

BASED ON THE STATUS BYTES[7:5] BITS, THE FOLLOWING STATISTICS ARE KEPT USING COUNTERS.

SLOT DEFINITION	STATISTICS	CALCULATION
DATA	1.NUMBER OF SLOTS 2.NUMBER OF SLOTS WITH POWER BUT NO DATA 3.NUMBER OF SLOTS WITH BAD DATA 4.NUMBER OF GOOD DATA-SLOTS 5.TOTAL NUMBER OF FEC BLOCKS 6.NUMBER OF FEC BLOCKS WITH CORRECTABLE ERRORS. 7.NUMBER OF UNCORRECTABLE FEC BLOCKS	NO UW UW AND (BAD FEC OR BAD HEC) UW AND GOOD HEC
REQUEST(CONTENTION)	1.NUMBER OF REQUESTS RECEIVED 2.NUMBER OF COLLIDED REQUESTS 3.NUMBER OF CORRUPTED REQUESTS	NO UW NO UW OR BAD FEC OR BAD HEC
REQUEST/DATA (CONTENTION)	1.NUMBER OF PACKETS RECEIVED 2.NUMBER OF COLLIDED PACKETS 3.NUMBER OF CORRUPTED PACKETS	NO UW NO UW OR BAD FEC OR BAD HEC
RANGING	1.NUMBER OF RANGING MESSAGES RECEIVED 2.NUMBER OF COLLIDED RANGING MESSAGES RECEIVED 3.NUMBER OF CORRUPTED RANGING MESSAGES	NO UW NO UW OR BAD FEC OR BAD HEC

FIG.55

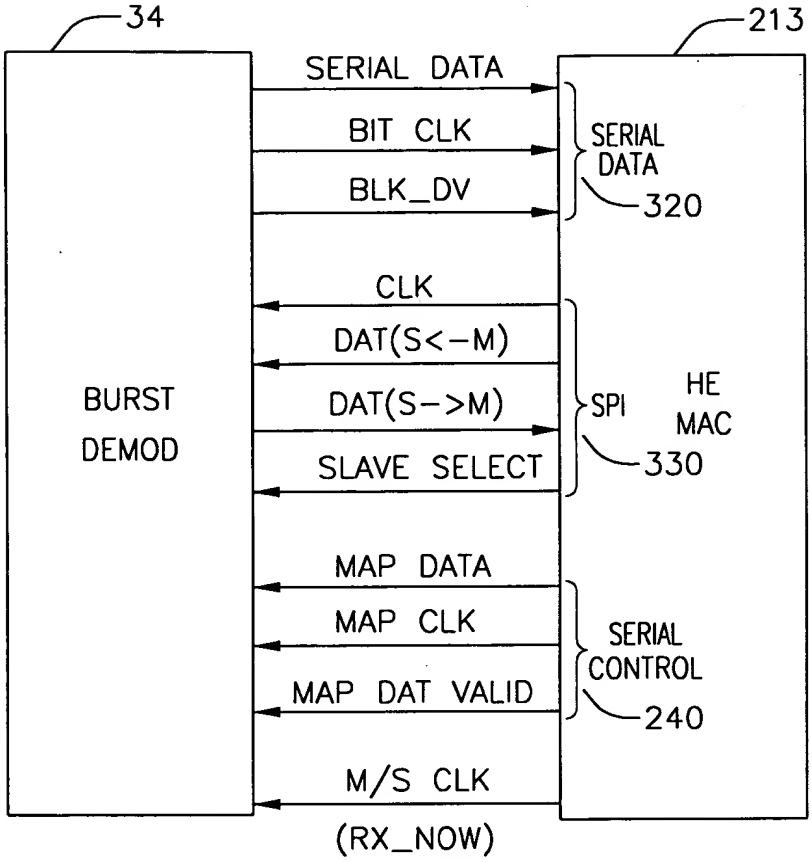

34
213
SERIAL DATA
BIT CLK
BLK_DV
SERIAL DATA
320
CLK
DAT(S<-M)
DAT(S->M)
SLAVE SELECT
SPI
HE MAC
330
BURST DEMOD
MAP DATA
MAP CLK
MAP DAT VALID
SERIAL CONTROL
240
M/S CLK
(RX_NOW)

FIG.56

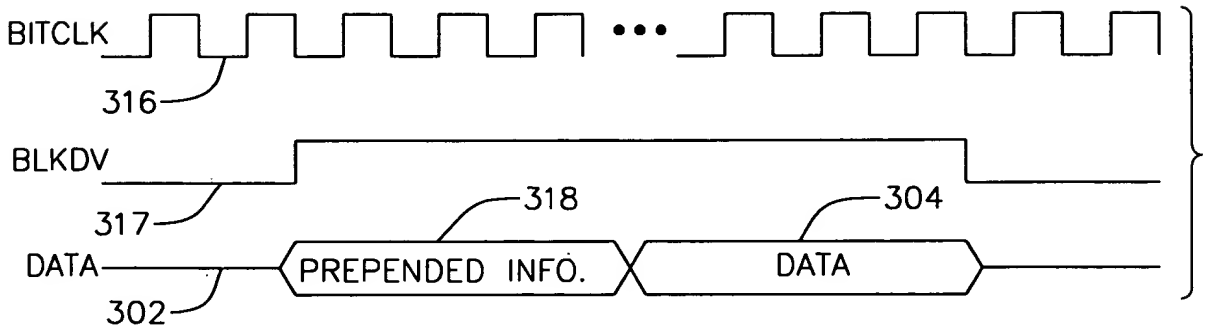

BITCLK
316
BLKDV
317
318
304
DATA
302
PREPENDED INFO.
DATA

FIG.57

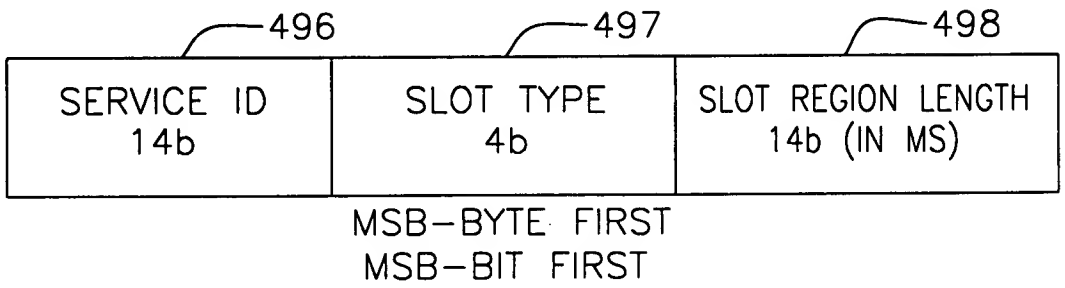


FIG.58

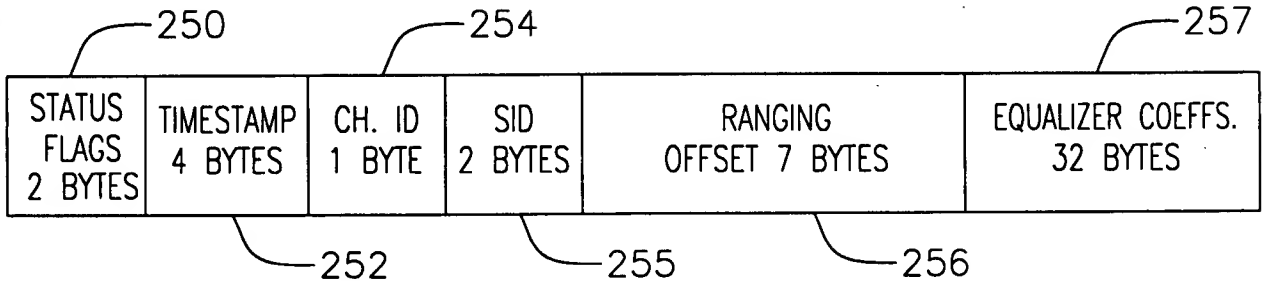


FIG.59

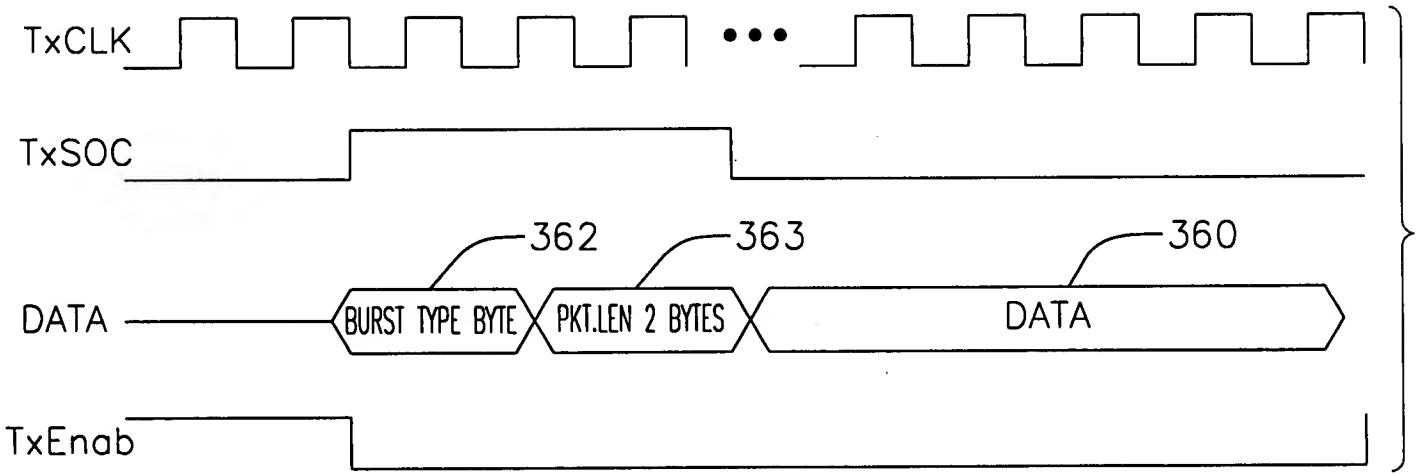
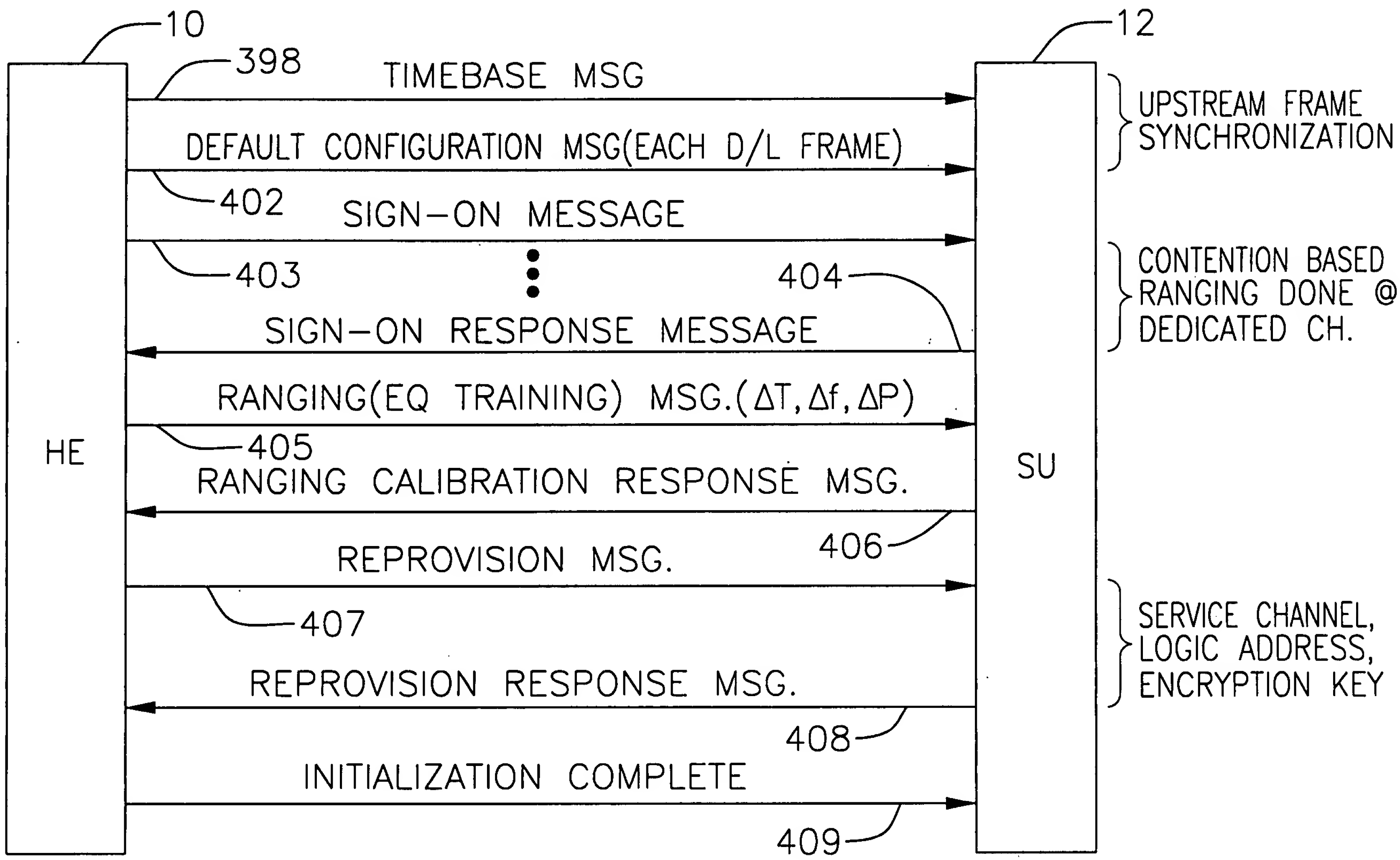


FIG.60



10
12
HE
SU
398
TIMEBASE MSG
DEFAULT CONFIGURATION MSG(EACH D/L FRAME)
402
SIGN–ON MESSAGE
403
404
SIGN–ON RESPONSE MESSAGE
RANGING(EQ TRAINING) MSG.(ΔT, Δf, ΔP)
405
RANGING CALIBRATION RESPONSE MSG.
406
REPROVISION MSG.
407
REPROVISION RESPONSE MSG.
408
INITIALIZATION COMPLETE
409
UPSTREAM FRAME SYNCHRONIZATION
CONTENTION BASED RANGING DONE @ DEDICATED CH.
SERVICE CHANNEL, LOGIC ADDRESS, ENCRYPTION KEY

FIG.61

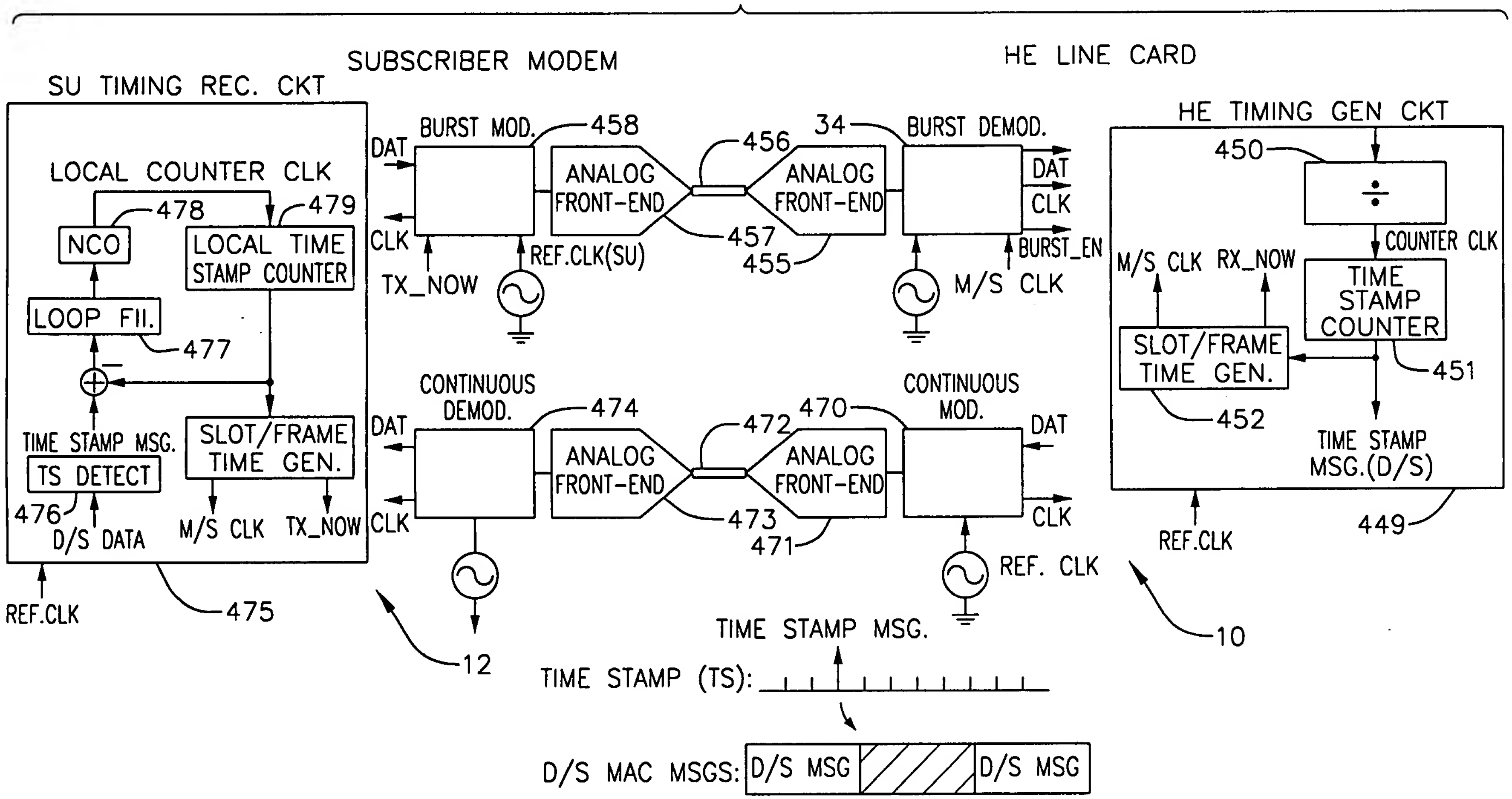

SUBSCRIBER MODEM
HE LINE CARD
SU TIMING REC. CKT
LOCAL COUNTER CLK
NCO
478
479
LOCAL TIME STAMP COUNTER
LOOP FIl.
477
TIME STAMP MSG.
TS DETECT
476
D/S DATA
SLOT/FRAME TIME GEN.
M/S CLK
TX_NOW
REF.CLK
475
BURST MOD.
458
DAT
CLK
TX_NOW
REF.CLK(SU)
ANALOG FRONT-END
456
457
455
34
BURST DEMOD.
DAT
CLK
BURST_EN
M/S CLK
CONTINUOUS DEMOD.
474
472
473
471
470
CONTINUOUS MOD.
REF. CLK
12
HE TIMING GEN CKT
450
COUNTER CLK
TIME STAMP COUNTER
451
M/S CLK
RX_NOW
SLOT/FRAME TIME GEN.
452
TIME STAMP MSG.(D/S)
REF.CLK
449
10
TIME STAMP MSG.
TIME STAMP (TS):
D/S MAC MSGS:
D/S MSG
D/S MSG

FIG.62

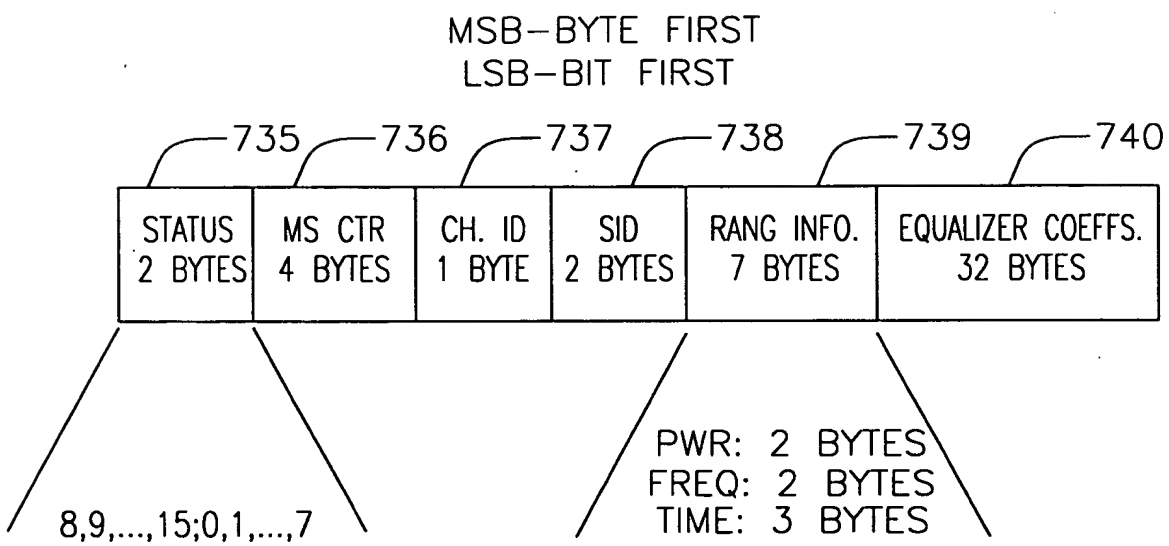

MSB–BYTE FIRST
LSB–BIT FIRST
735
736
737
738
739
740
STATUS
2 BYTES
MS CTR
4 BYTES
CH. ID
1 BYTE
SID
2 BYTES
RANG INFO.
7 BYTES
EQUALIZER COEFFS.
32 BYTES
8,9,...,15;0,1,...,7
PWR: 2 BYTES
FREQ: 2 BYTES
TIME: 3 BYTES

FIG.63

BIT FIELD	DEFINITION IF BIT[11]=1	DEFINITION IF BIT[11]=0
BIT[15:12]	DOCSIS IUC	RESERVED
BIT[11]	1:INDICATES 1ST. BLOCK OF TRANSMISSION	0:INDICATES NOT 1ST. BLOCK OF TRANSMISSION
BIT[10]	1:INDICATES LAST BLOCK OF TRANSMISSION	1:INDICATES LAST BLOCK OF TRANSMISSION
BIT[9]	1:INDICATES RANGING REQUIRED	RESERVED
BIT[8]	RESERVED	RESERVED
BIT[7:5]	000:FEC OK 001:CORRECTABLE FEC ERROR 010:UNCORRECTABLE FEC ERROR 011:NO UNIQUE WORD DETECTED 100:COLLIDED PACKET 101:NO ENERGY 110:PACKET LENGTH VIOLATION	000:FEC OK 001:CORRECTABLE FEC ERROR 010:UNCORRECTABLE FEC ERROR 011:NO UNIQUE WORD DETECTED 100:COLLIDED PACKET 101:NO ENERGY 110:PACKET LENGTH VIOLATION
BIT[4]	1:VALID MINISLOT COUNT PREPENDED	RESERVED
BIT[3]	1:VALID CHANNEL ID PREPENDED	RESERVED
BIT[2]	1:VALID SID PREPENDED	RESERVED
BIT[1]	1:RANGING INFO PREPENDED	RESERVED
BIT[0]	1:EQUALIZER COEFFICIENTS PREPENDED	RESERVED

FIG.64

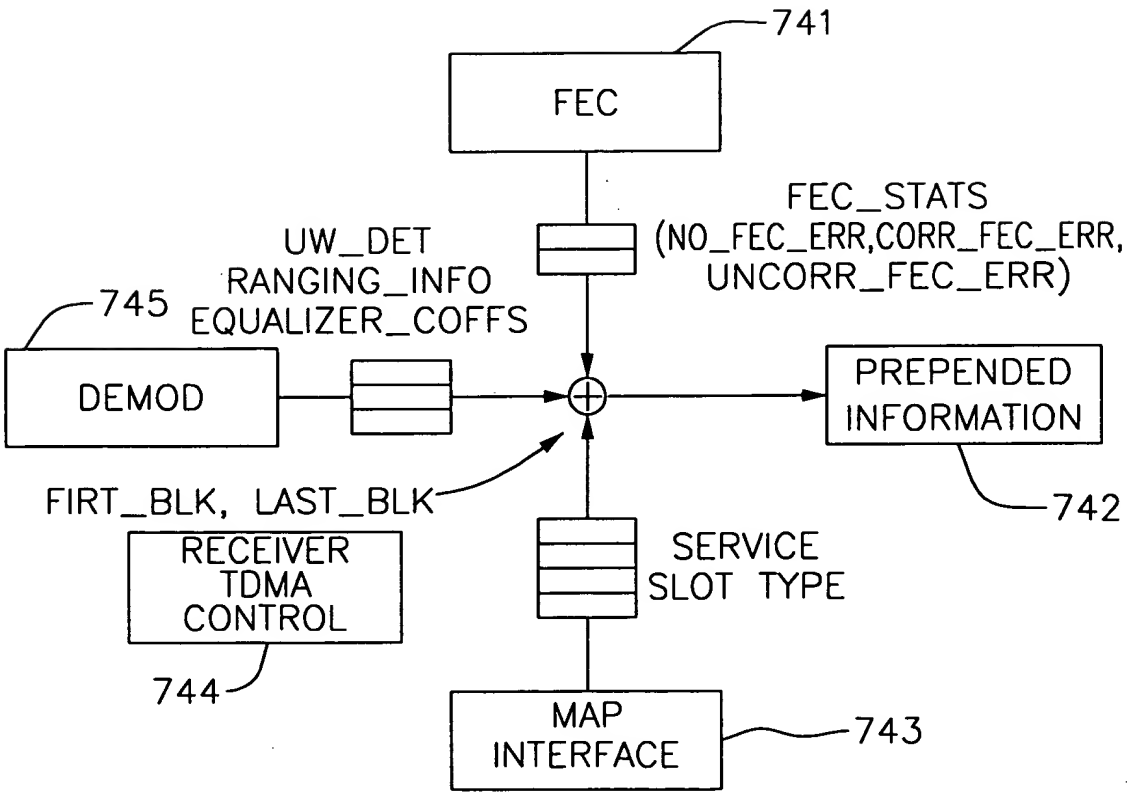

741
FEC
FEC_STATS
(NO_FEC_ERR,CORR_FEC_ERR,
UNCORR_FEC_ERR)
UW_DET
RANGING_INFO
EQUALIZER_COFFS
745
DEMOD
PREPENDED
INFORMATION
742
FIRT_BLK, LAST_BLK
RECEIVER
TDMA
CONTROL
744
SERVICE
SLOT TYPE
MAP
INTERFACE
743

FIG.65

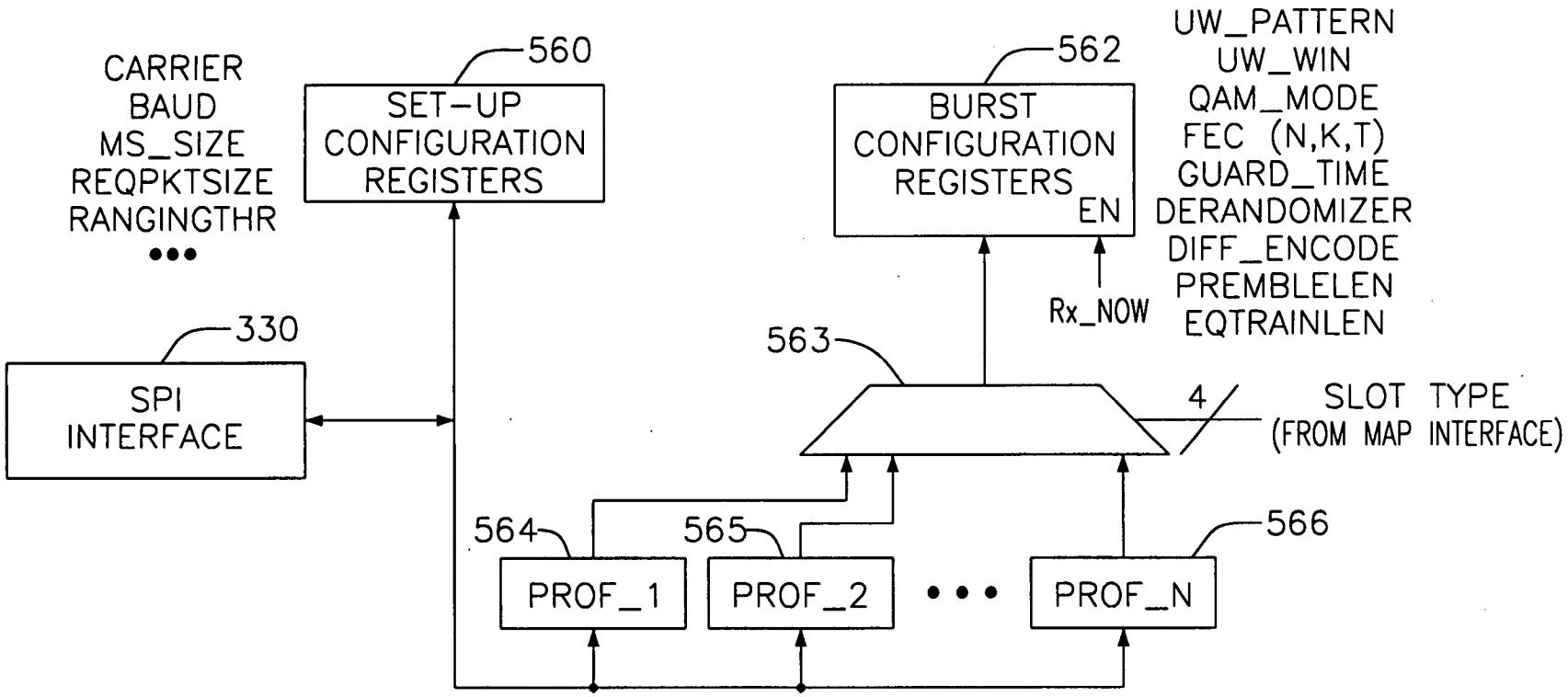
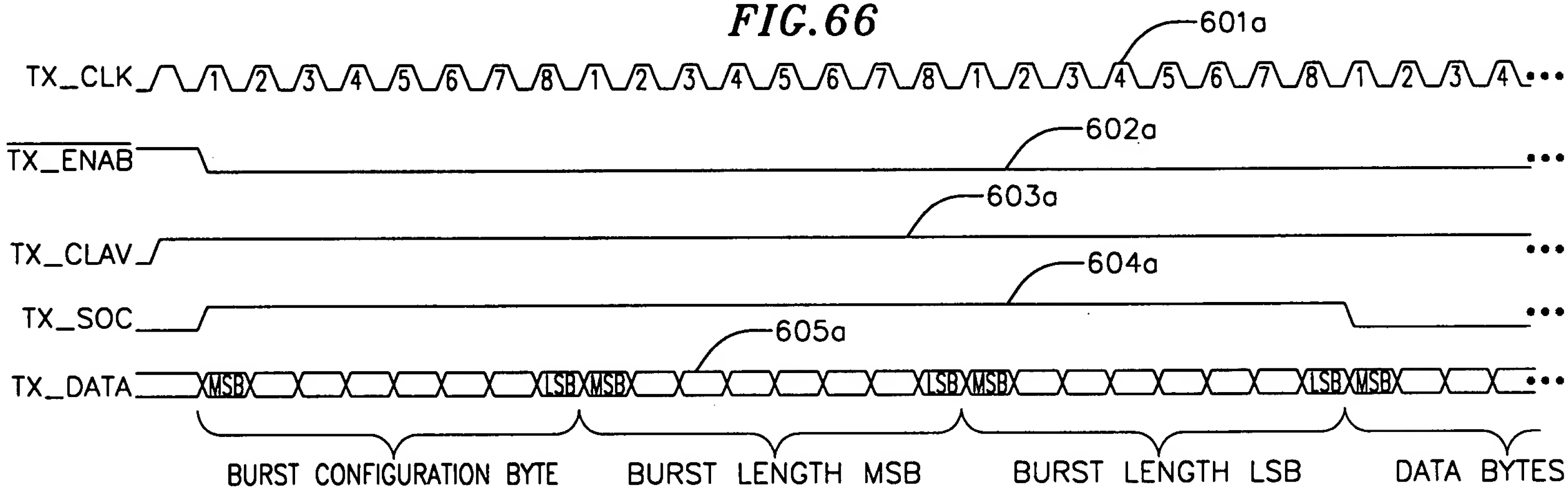
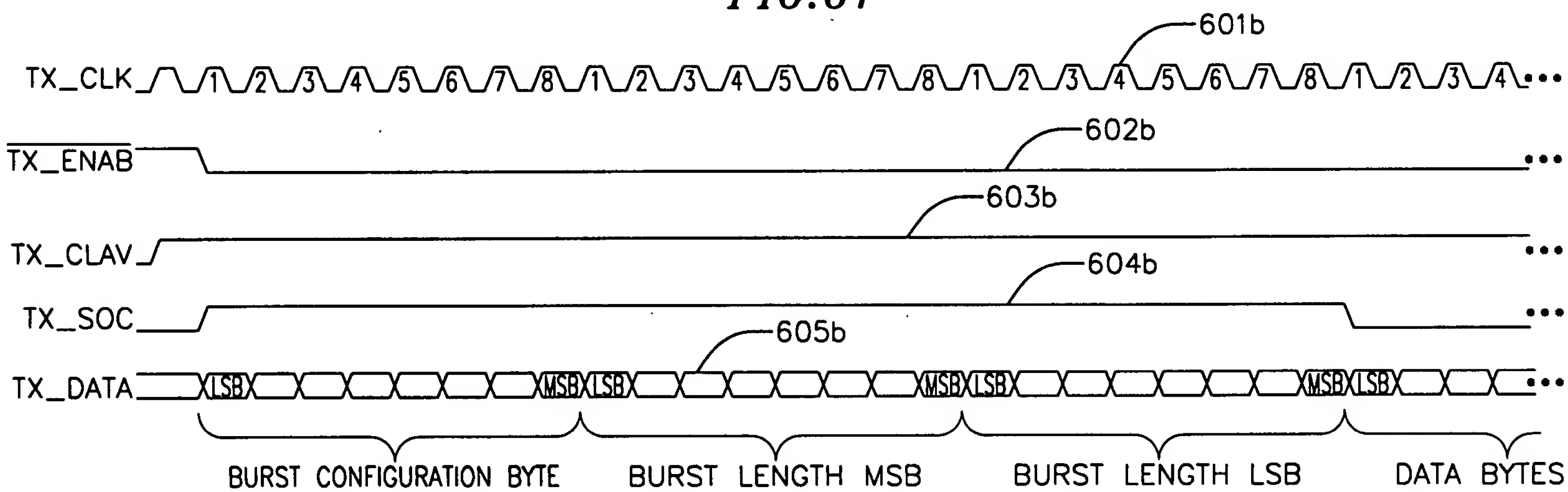

CARRIER
BAUD
MS_SIZE
REQPKTSIZE
RANGINGTHR
•••
560
SET-UP
CONFIGURATION
REGISTERS
330
SPI
INTERFACE
562
BURST
CONFIGURATION
REGISTERS
EN
UW_PATTERN
UW_WIN
QAM_MODE
FEC (N,K,T)
GUARD_TIME
DERANDOMIZER
DIFF_ENCODE
PREMBLELEN
EQTRAINLEN
Rx_NOW
563
4
SLOT TYPE
(FROM MAP INTERFACE)
564
565
566
PROF_1
PROF_2
• • •
PROF_N

FIG.66



601a
602a
603a
604a
605a
TX_CLK
TX_ENAB
TX_CLAV
TX_SOC
TX_DATA
MSB
LSB
BURST CONFIGURATION BYTE
BURST LENGTH MSB
BURST LENGTH LSB
DATA BYTES

FIG.67



601b
602b
603b
604b
605b
TX_CLK
TX_ENAB
TX_CLAV
TX_SOC
TX_DATA
LSB
MSB
BURST CONFIGURATION BYTE
BURST LENGTH MSB
BURST LENGTH LSB
DATA BYTES

FIG.68

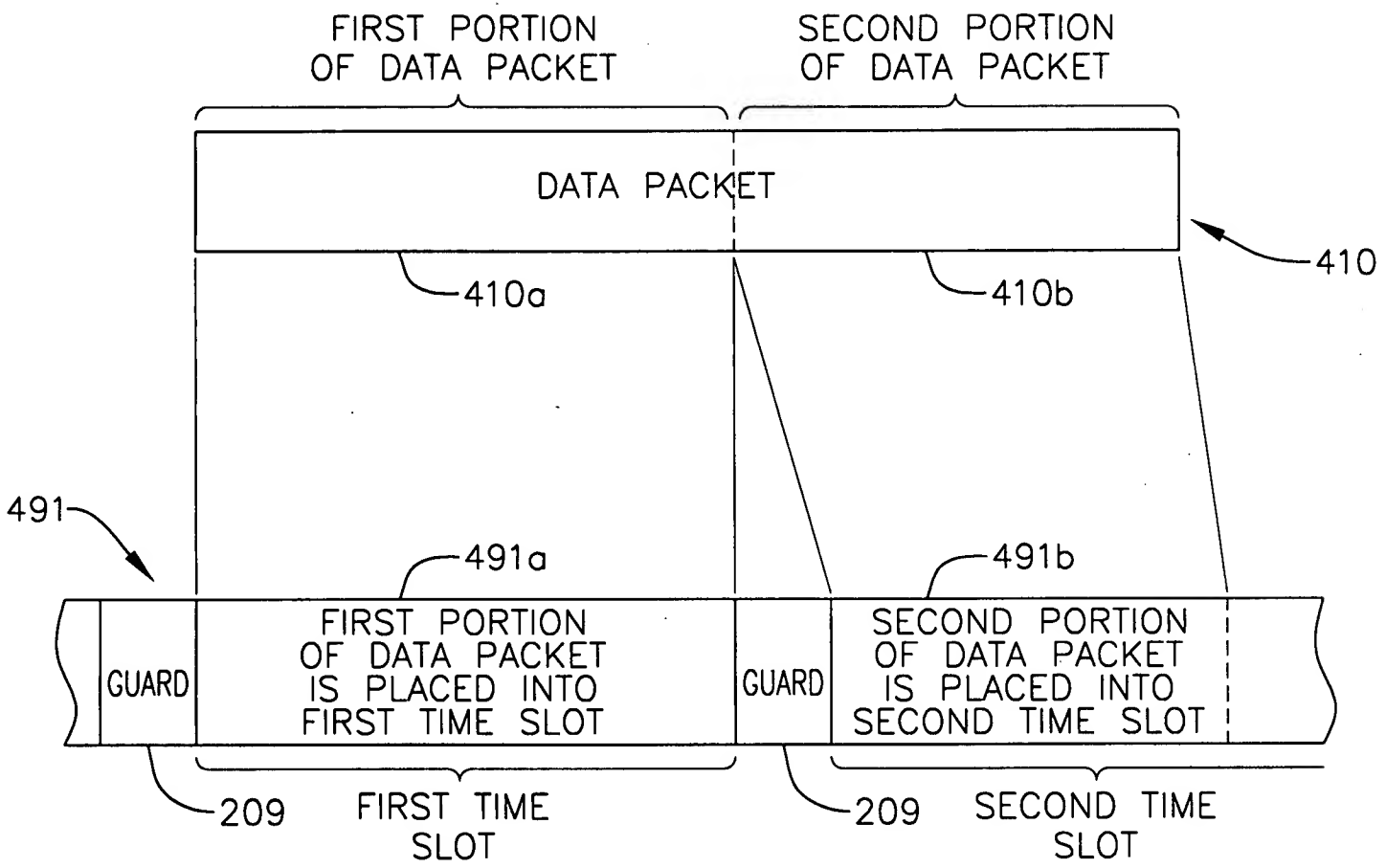

FIRST PORTION OF DATA PACKET
SECOND PORTION OF DATA PACKET
DATA PACKET
410
410a
410b
491
491a
491b
GUARD
FIRST PORTION OF DATA PACKET IS PLACED INTO FIRST TIME SLOT
GUARD
SECOND PORTION OF DATA PACKET IS PLACED INTO SECOND TIME SLOT
209
FIRST TIME SLOT
209
SECOND TIME SLOT

FIG.69

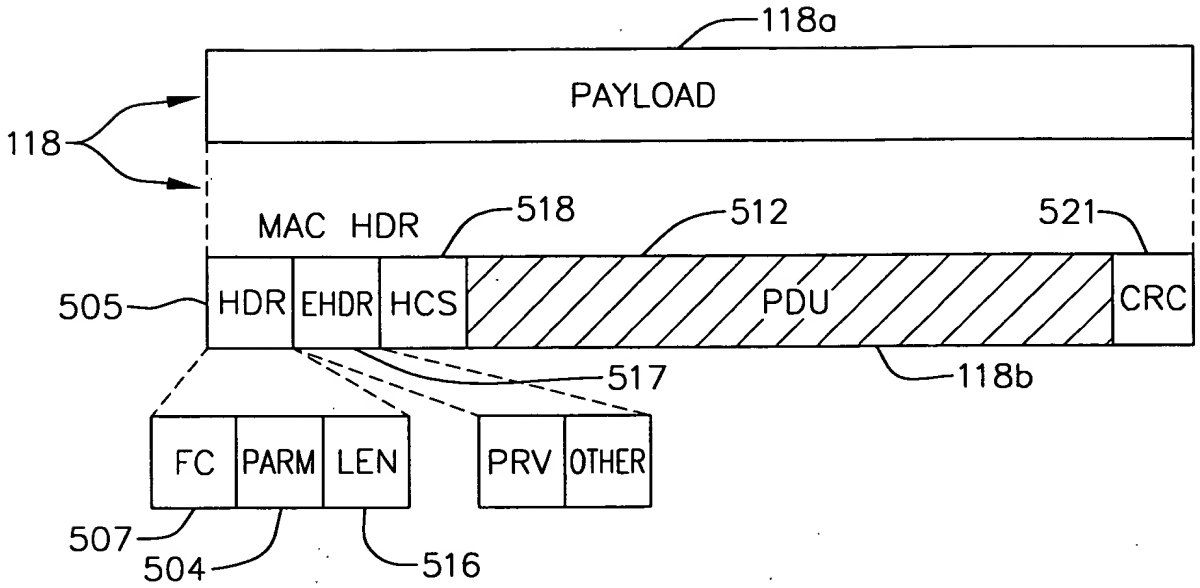

118a
PAYLOAD
118
MAC HDR
518
512
521
505
HDR
EHDR
HCS
PDU
CRC
517
118b
FC
PARM
LEN
PRV
OTHER
507
504
516

FIG.70

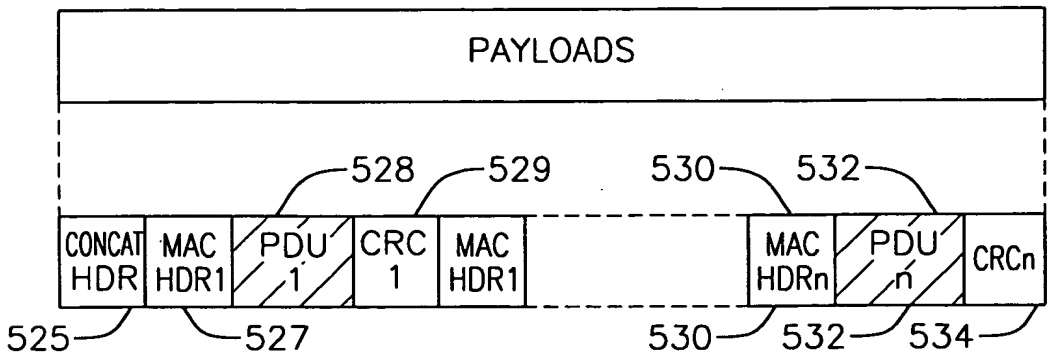

PAYLOADS
528
529
530
532
CONCAT HDR
MAC HDR1
PDU 1
CRC 1
MAC HDR1
MAC HDRn
PDU n
CRCn
525
527
530
532
534

FIG. 71

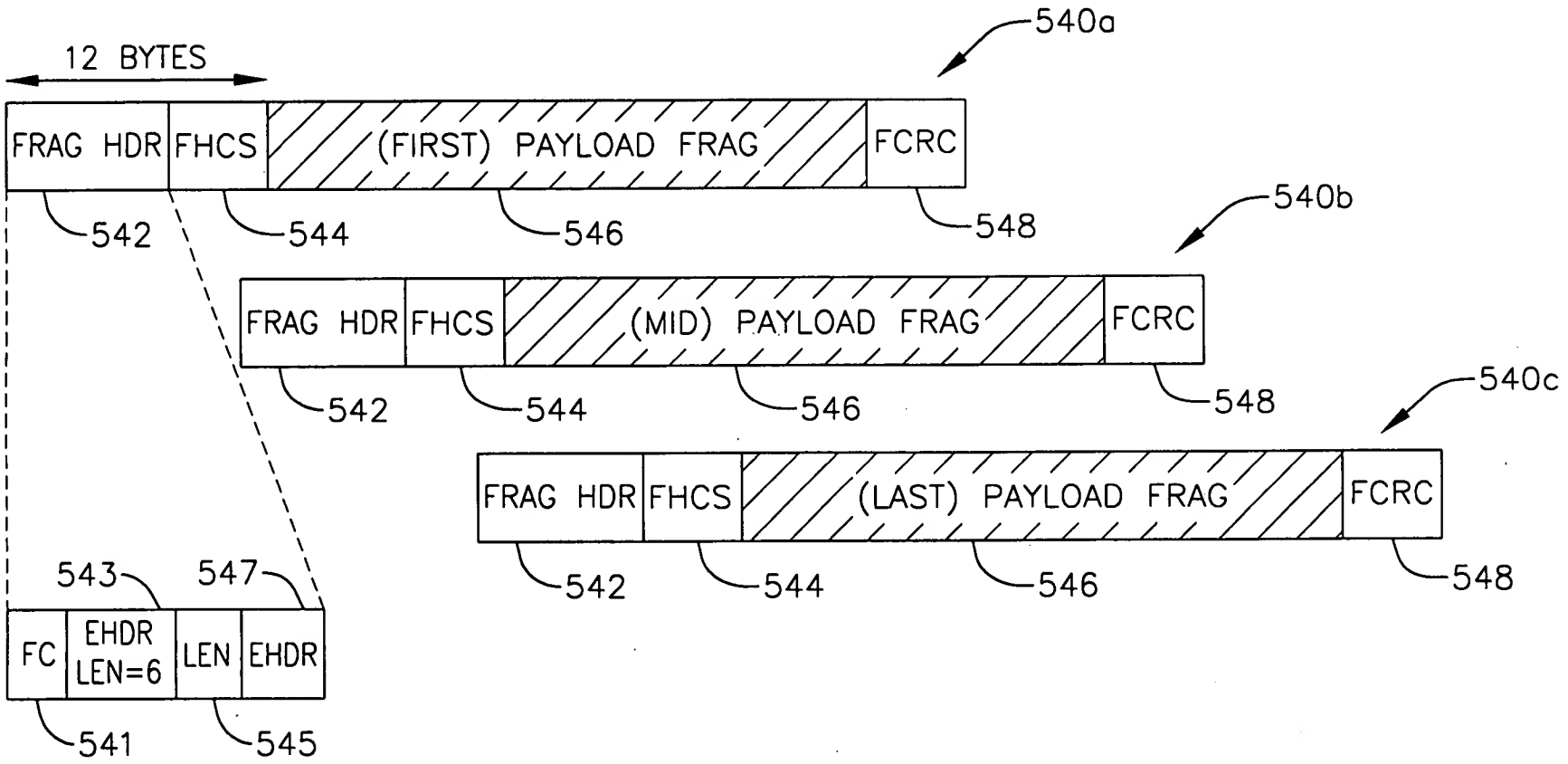

12 BYTES
540a
FRAG HDR
FHCS
(FIRST) PAYLOAD FRAG
FCRC
542
544
546
548
540b
FRAG HDR
FHCS
(MID) PAYLOAD FRAG
FCRC
542
544
546
548
540c
FRAG HDR
FHCS
(LAST) PAYLOAD FRAG
FCRC
542
544
546
548
543
547
FC
EHDR LEN=6
LEN
EHDR
541
545

FIG. 72

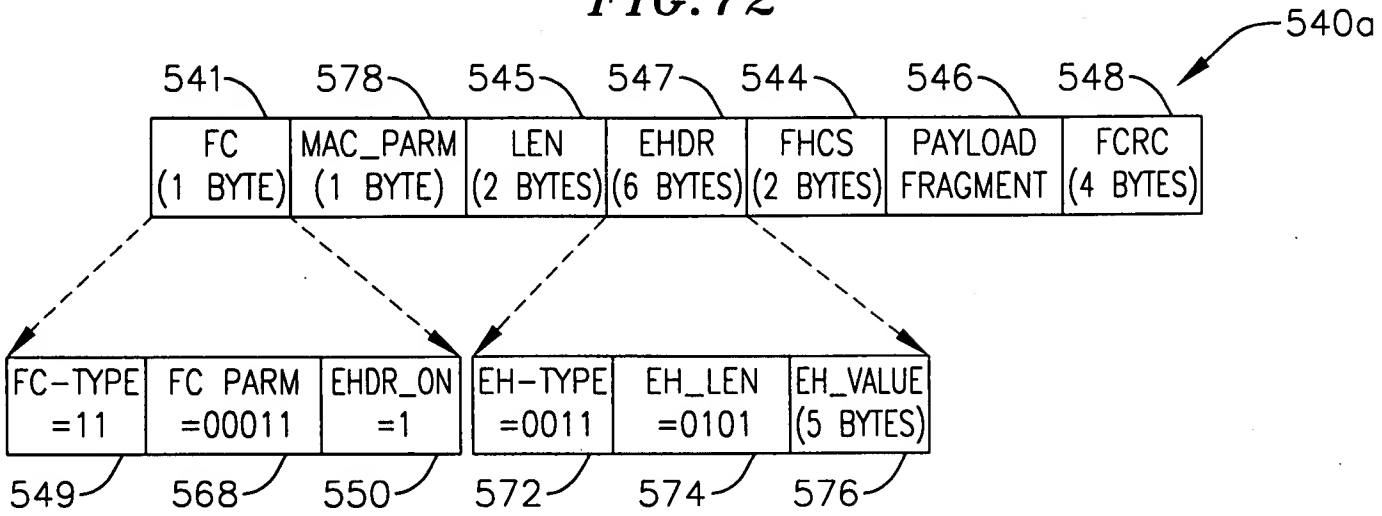


FIG. 73

FIELD	USAGE	SIZE
FC	FC_TYPE=11;MAC-SPECIFIC HEADER FC_PARM [4:0]=00011;FRAGMENTATION MAC HEADER EHDR_ON = 1;FRAGMENTATION EHDR FOLLOWS	8 BITS
MAC_PARM	ELEN = 6 BYTES;LENGTH OF FRAGMENTATION EHDR	8 BITS
LEN	LEN = n+10;TOTAL LENGTH OF THIS FRAGMENT INCLUDING PAYLOAD, EHDR, FCRC	16 BITS

FIG.74

FIELD	USAGE	SIZE	
EHDR	EH_TYPE=3;SAME TYPE AS BP_UP EH_LEN=5;LENGTH OF THIS EHDR KEY_SEQ;SAME AS IN BP_UP VER=0001;VERSION NUMBER FOR THIS EHDR ENABLE IF ENABLE=0, BPI DISABLED IF ENABLE=1, BPI ENABLED TOGGLE BIT;SAME AS IN BP_UP SID;SERVICE ID ASSOCIATED WITH THIS FRAGMENT REQ;NUMBER OF MINI-SLOTS FOR A PIGGYBACK REQUEST RESERVED;MUST BE SET TO ZERO FIRST_FRAG;SET TO ONE FOR FIRST FRAGMENT ONLY LAST_FRAG;SET TO ONE FOR LAST FRAGMENT ONLY FRAG_SEQ;FRAGMENT SEQUENCE COUNT, INCREMENTED FOR EACH FRAGMENT, SET TO ZERO FOR FIRST FRAGMENT	4 BITS 4 BITS 4 BITS 4 BITS 1 BIT 1 BIT 14 BITS 8 BITS 2 BITS 1 BIT 1 BIT 4 BITS	6 BYTES
FHCS	MAC HEADER CHECK SEQUENCE		2 BYTES
PAYLOAD	FRAGMENT PAYLOAD;PORTION OF TOTAL MAC PDU BEING SENT		n BYTES
FCRC	CRC ACROSS FRAGMENT PAYLOAD		4 BYTES
	LENGTH OF A MAC FRAGMENT FRAME	n + 16 BYTES	

FIG.75

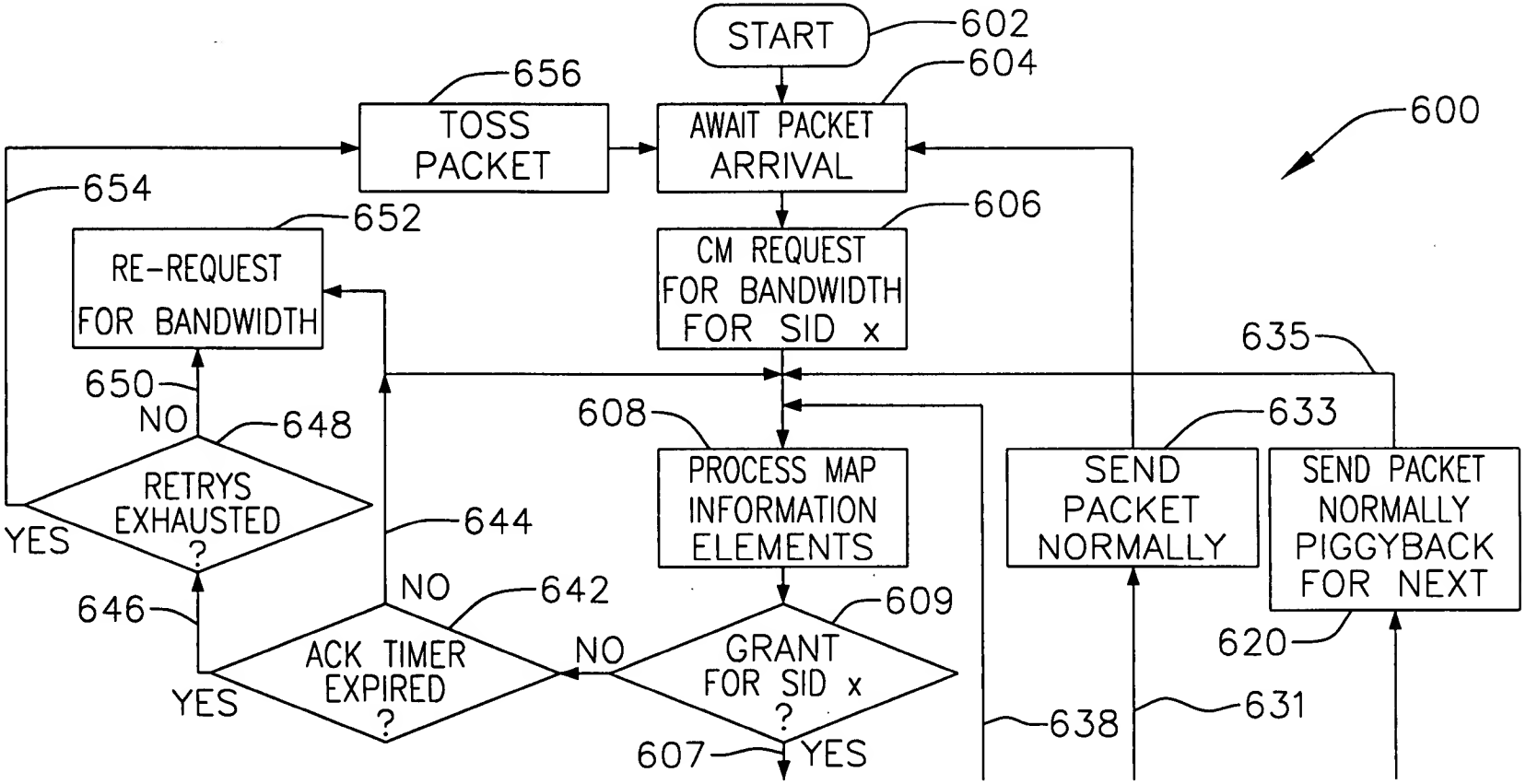

START
602
604
600
656
TOSS PACKET
AWAIT PACKET ARRIVAL
654
652
606
RE-REQUEST FOR BANDWIDTH
CM REQUEST FOR BANDWIDTH FOR SID x
635
650
NO
648
608
633
RETRYS EXHAUSTED ?
PROCESS MAP INFORMATION ELEMENTS
SEND PACKET NORMALLY
SEND PACKET NORMALLY PIGGYBACK FOR NEXT
YES
644
NO
642
609
646
620
ACK TIMER EXPIRED ?
NO
GRANT FOR SID x ?
638
631
YES
607
YES

FIG. 76

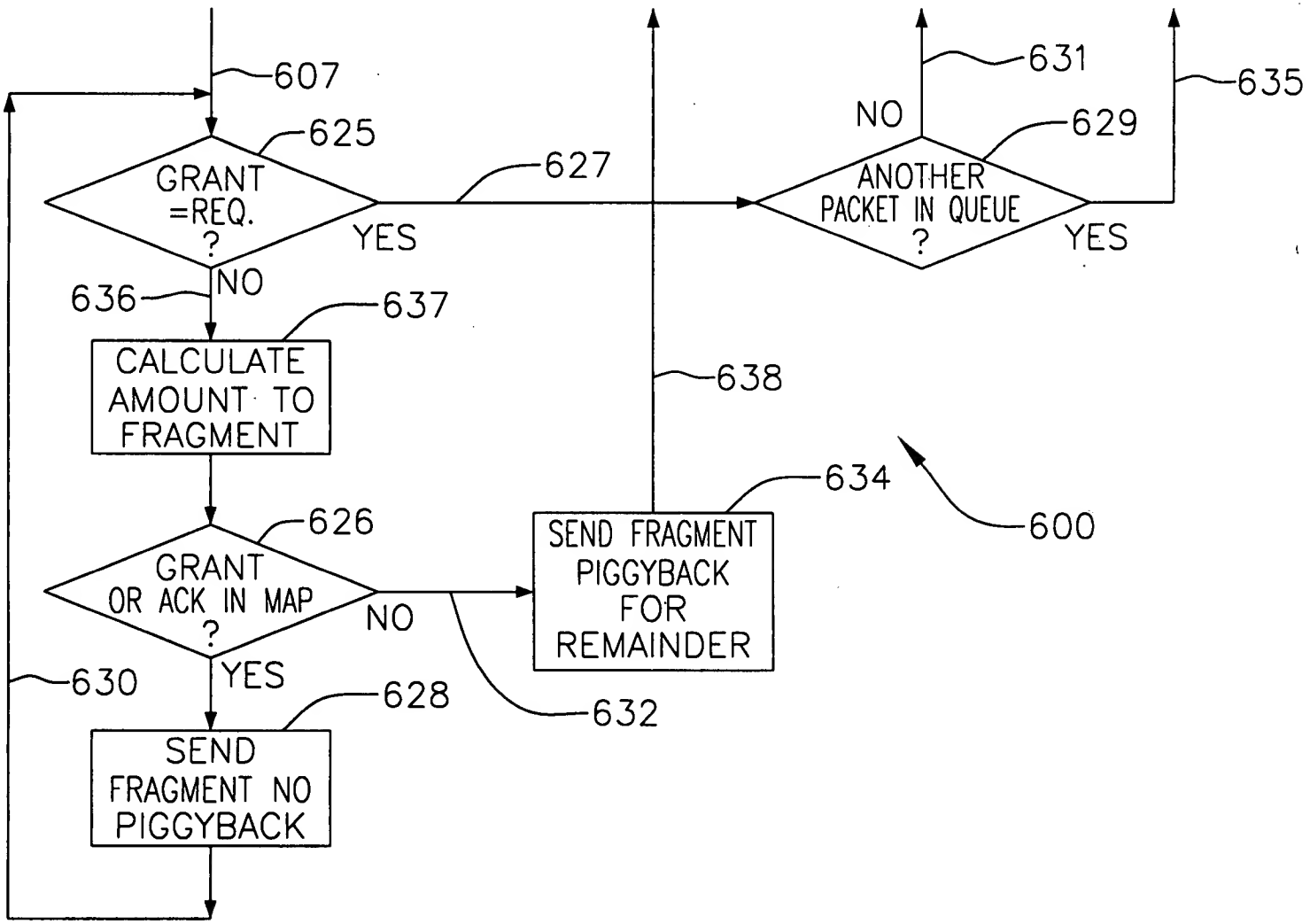

607
625
GRANT =REQ. ?
YES
627
NO
631
635
629
ANOTHER PACKET IN QUEUE ?
YES
636
NO
637
CALCULATE AMOUNT TO FRAGMENT
638
634
600
626
GRANT OR ACK IN MAP ?
NO
SEND FRAGMENT PIGGYBACK FOR REMAINDER
630
YES
628
632
SEND FRAGMENT NO PIGGYBACK

FIG.77

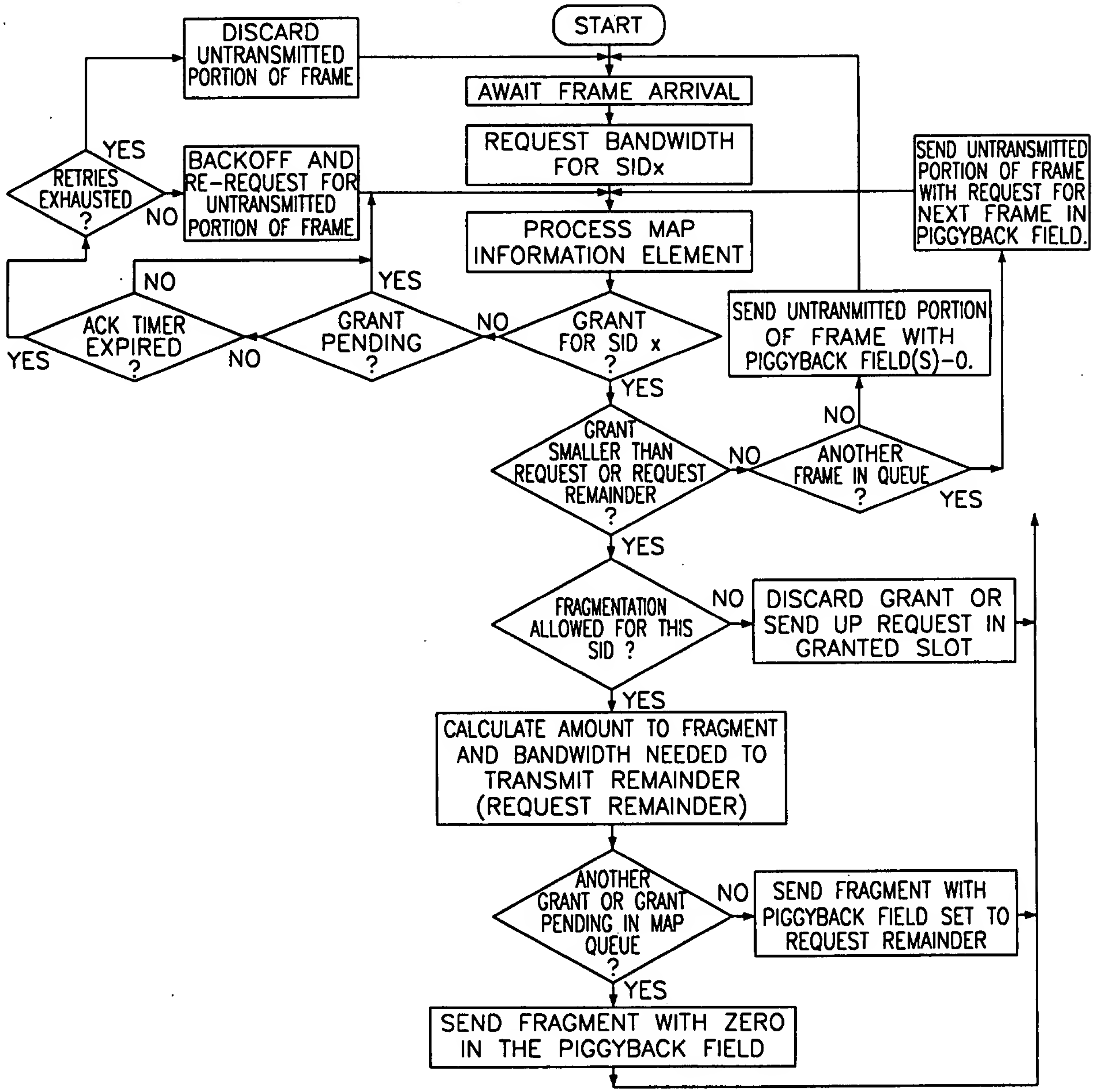


FIG. 78

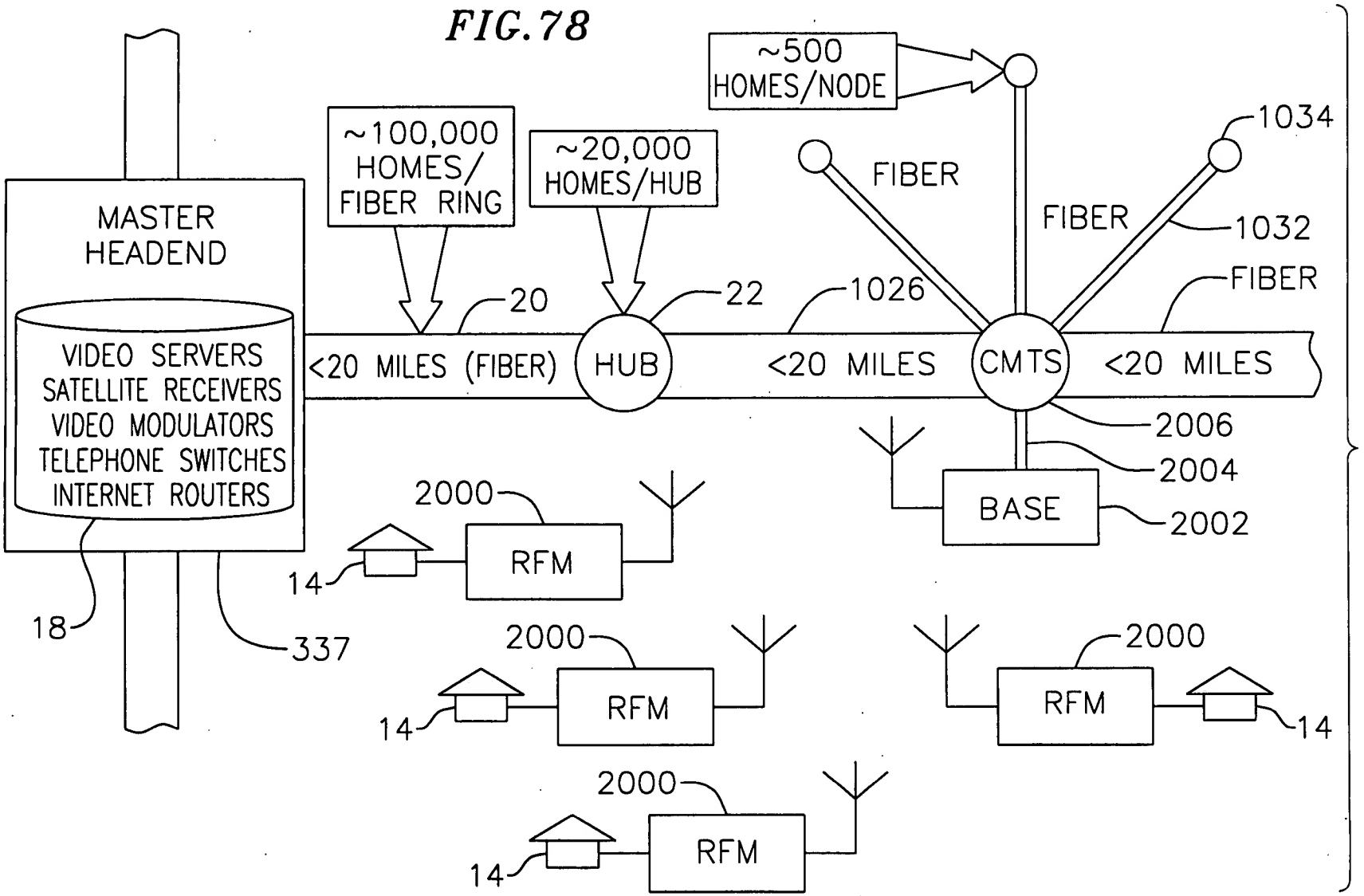

MASTER HEADEND
VIDEO SERVERS
SATELLITE RECEIVERS
VIDEO MODULATORS
TELEPHONE SWITCHES
INTERNET ROUTERS
18
337
~100,000 HOMES/ FIBER RING
~20,000 HOMES/HUB
~500 HOMES/NODE
20
22
1026
1034
1032
FIBER
FIBER
FIBER
<20 MILES (FIBER)
HUB
<20 MILES
CMTS
<20 MILES
2006
2004
BASE
2002
2000
RFM
14
2000
RFM
14
2000
RFM
14
2000
RFM
14

FIG.79

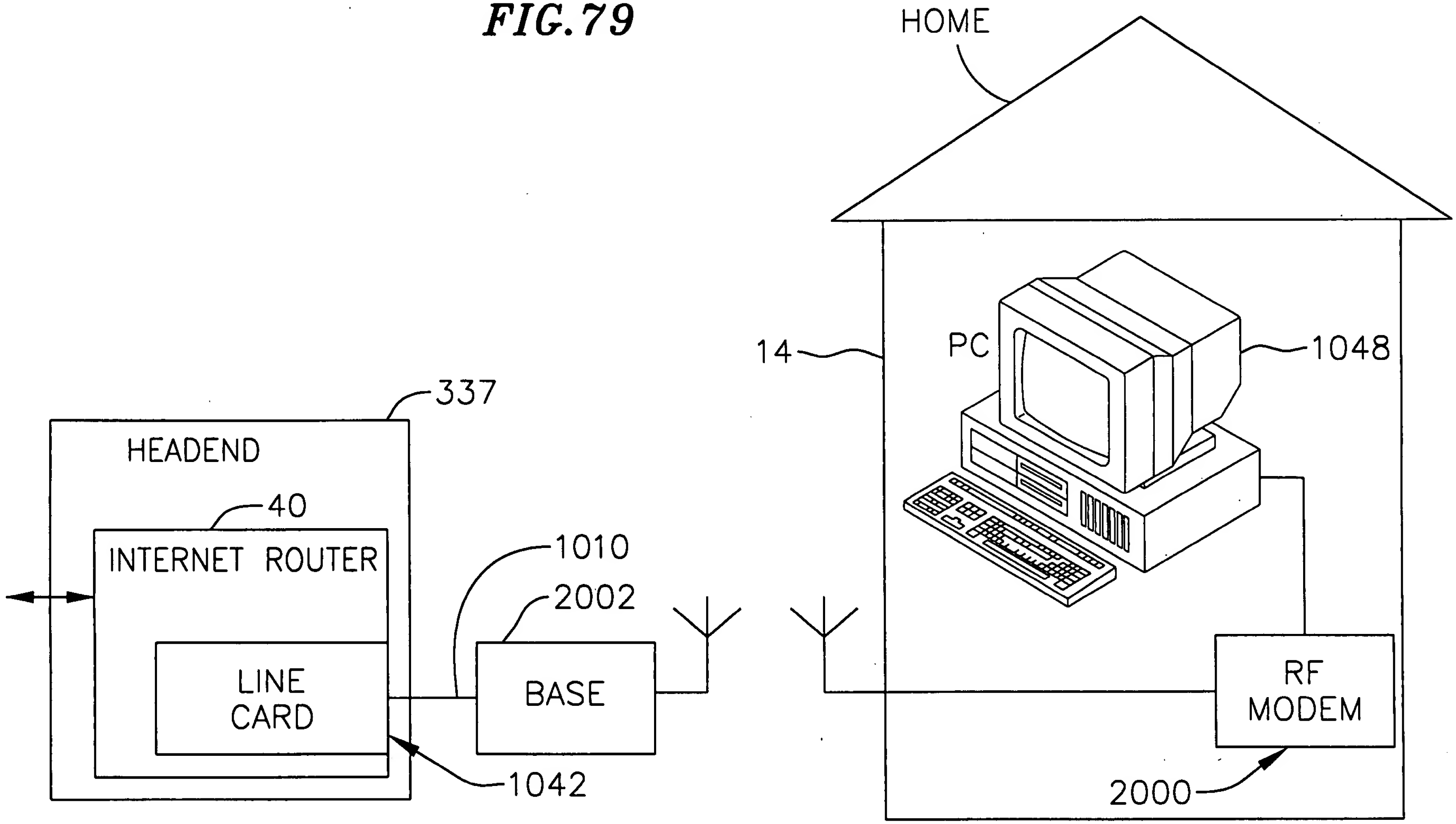


FIG.80

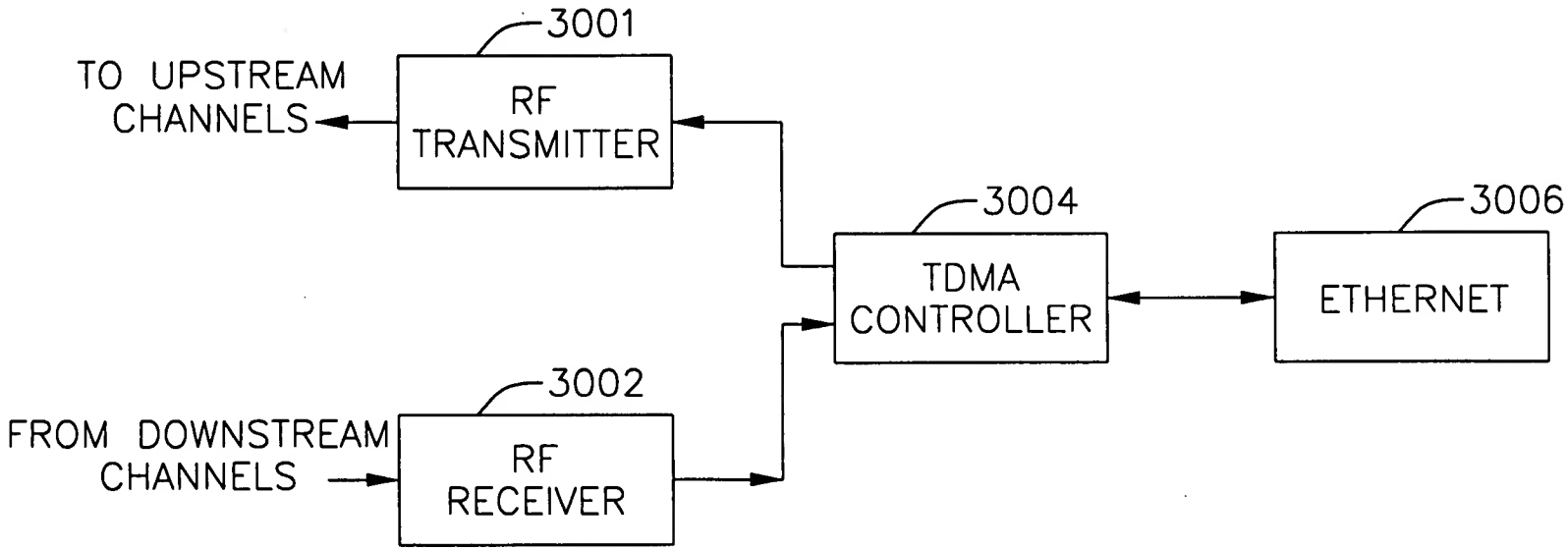

3001
TO UPSTREAM CHANNELS
RF TRANSMITTER
3004
TDMA CONTROLLER
3006
ETHERNET
3002
FROM DOWNSTREAM CHANNELS
RF RECEIVER

FIG.81

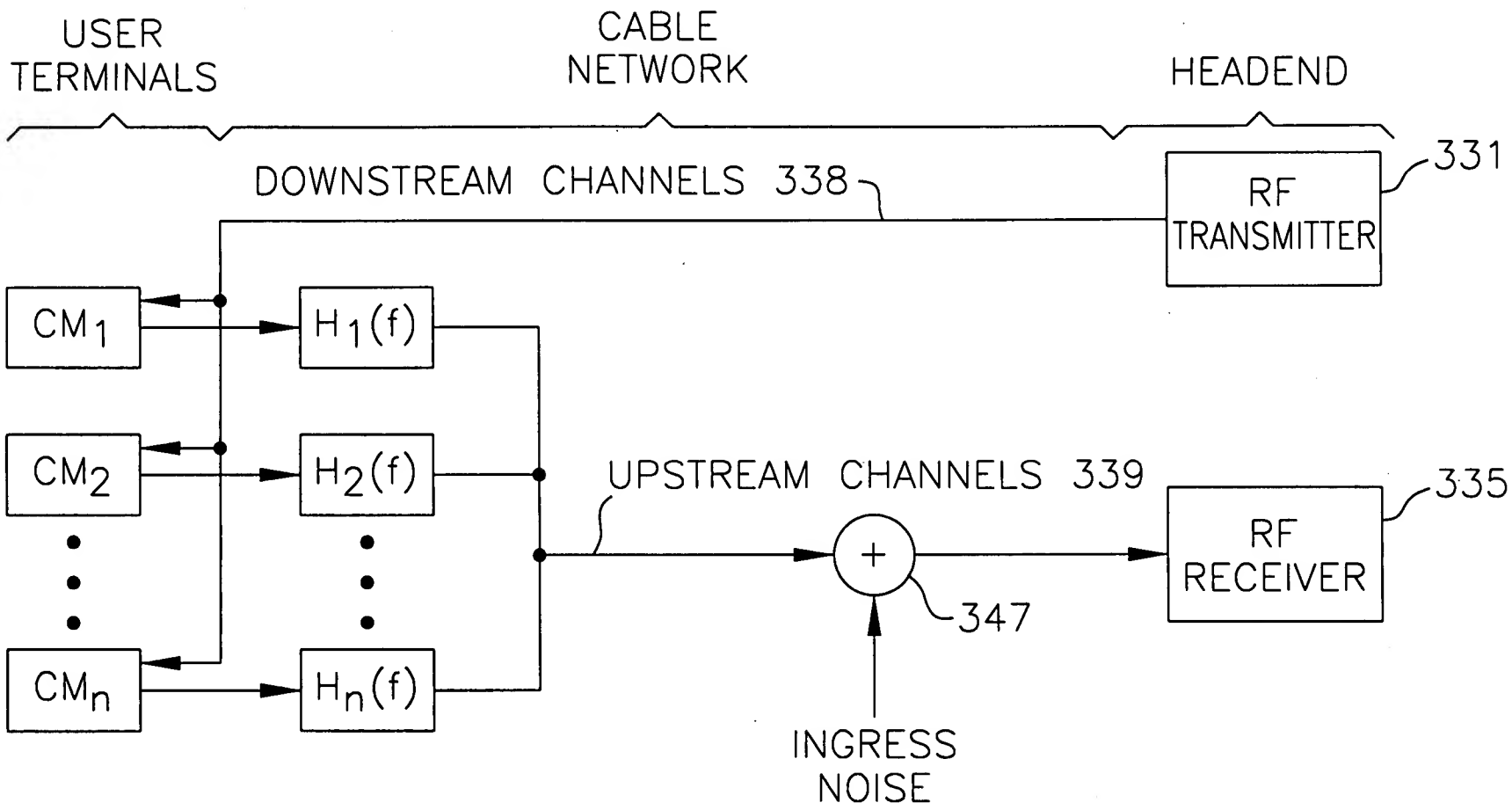

USER TERMINALS
CABLE NETWORK
HEADEND
DOWNSTREAM CHANNELS 338
331
RF TRANSMITTER
CM1
CM2
CMn
H1(f)
H2(f)
Hn(f)
UPSTREAM CHANNELS 339
335
RF RECEIVER
+
347
INGRESS NOISE

FIG.82

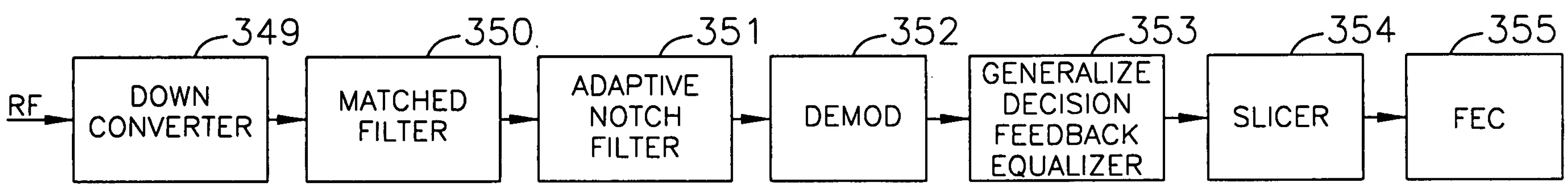

RF
349
DOWN CONVERTER
350
MATCHED FILTER
351
ADAPTIVE NOTCH FILTER
352
DEMOD
353
GENERALIZE DECISION FEEDBACK EQUALIZER
354
SLICER
355
FEC

FIG.83

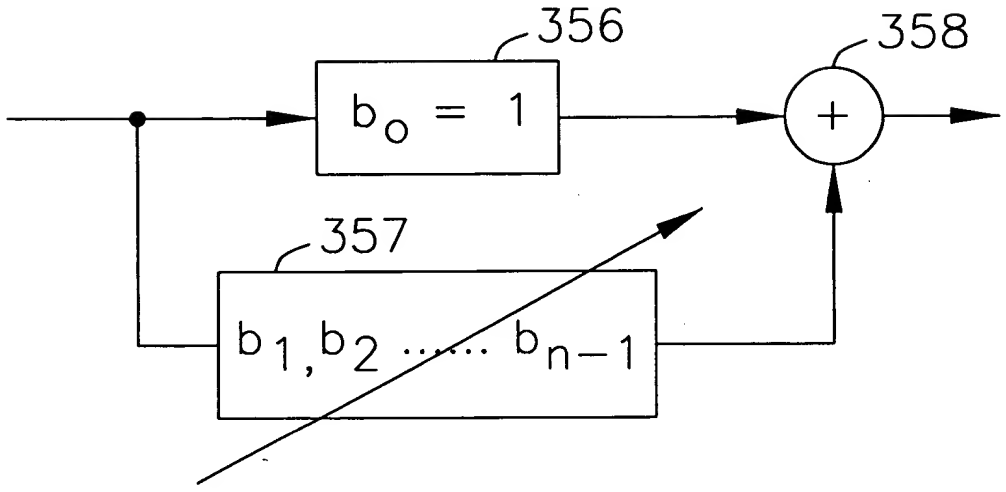

356
358
$b_o = 1$
+
357
$b_1, b_2 \ldots\ldots b_{n-1}$

FIG.84

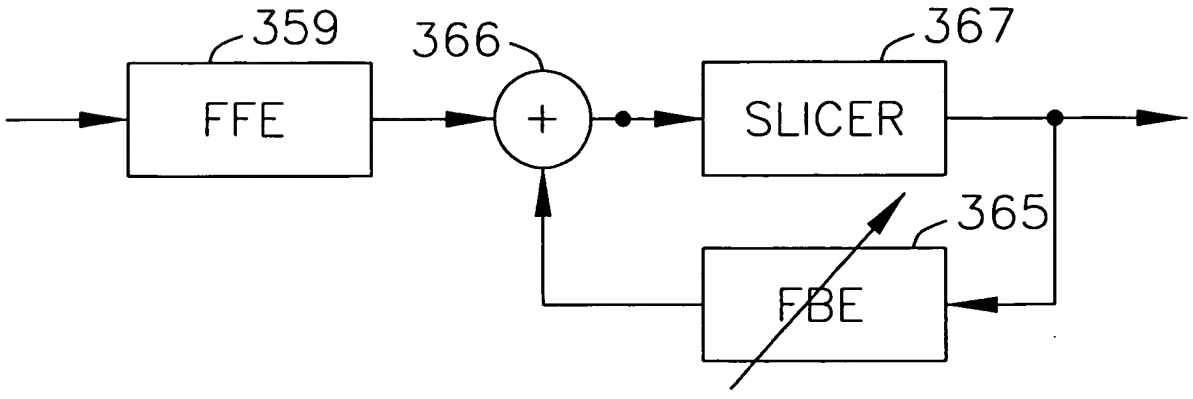

359
366
367
FFE
+
SLICER
365
FBE

FIG.85

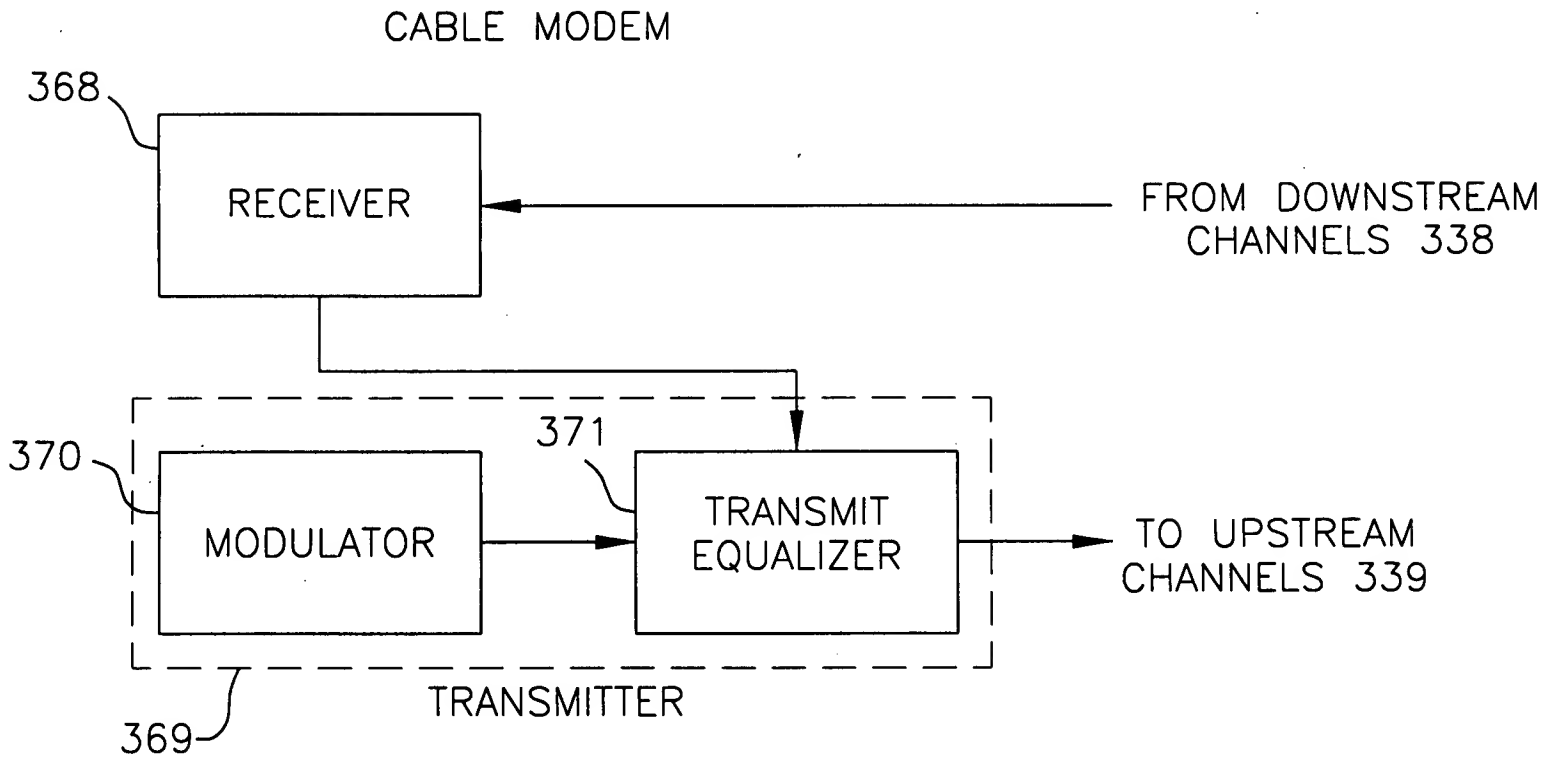

CABLE MODEM
368
RECEIVER
FROM DOWNSTREAM CHANNELS 338
371
370
MODULATOR
TRANSMIT EQUALIZER
TO UPSTREAM CHANNELS 339
TRANSMITTER
369

FIG.86

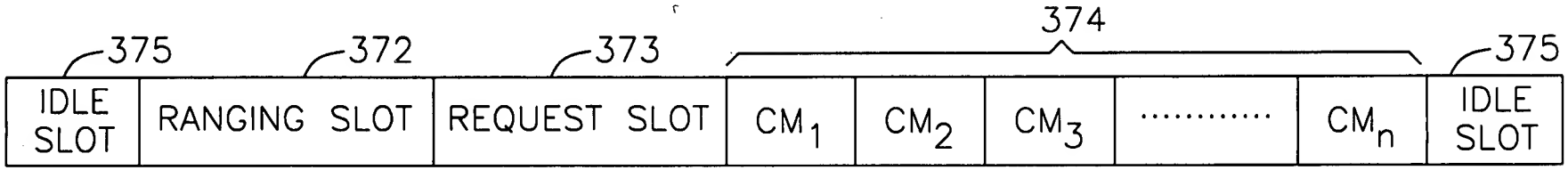

375
372
373
374
375
IDLE SLOT
RANGING SLOT
REQUEST SLOT
CM1
CM2
CM3
.....
CMn
IDLE SLOT

FIG.87

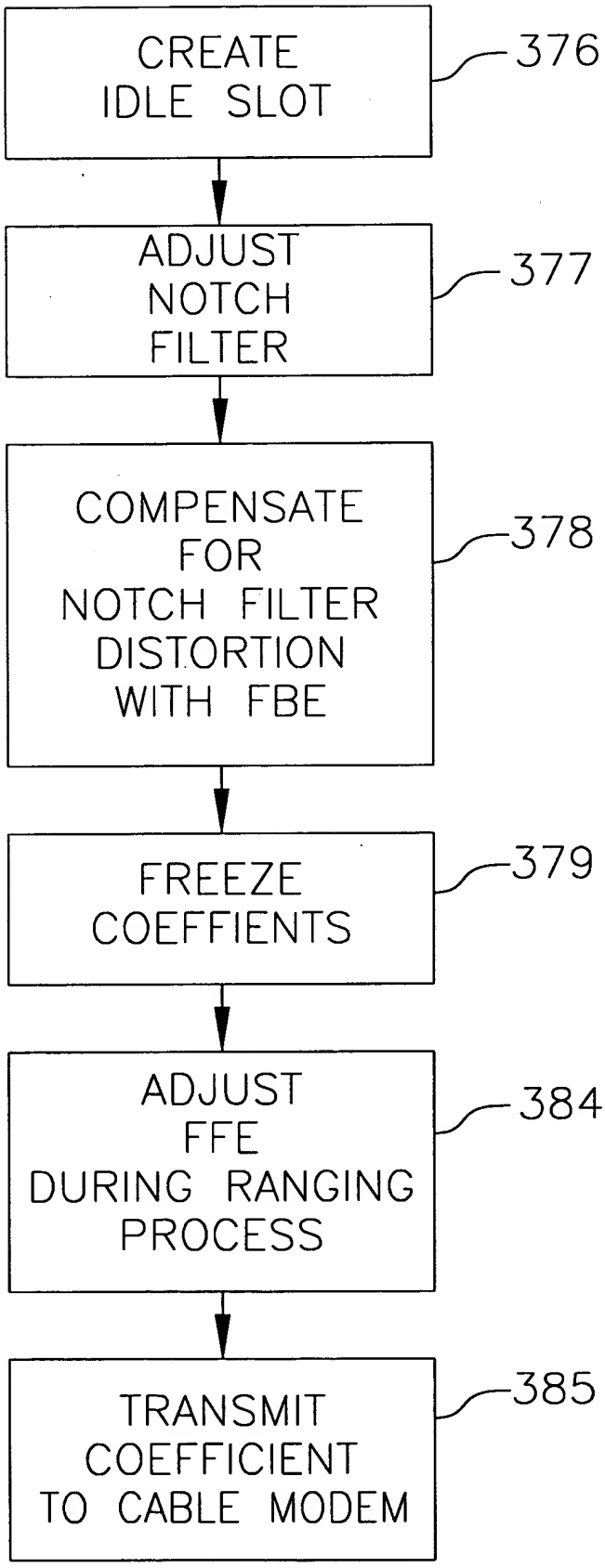

CREATE IDLE SLOT
376
ADJUST NOTCH FILTER
377
COMPENSATE FOR NOTCH FILTER DISTORTION WITH FBE
378
FREEZE COEFFIENTS
379
ADJUST FFE DURING RANGING PROCESS
384
TRANSMIT COEFFICIENT TO CABLE MODEM
385

FIG.88A

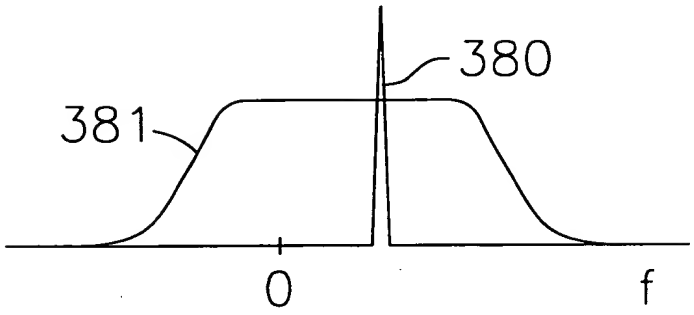


FIG.88B

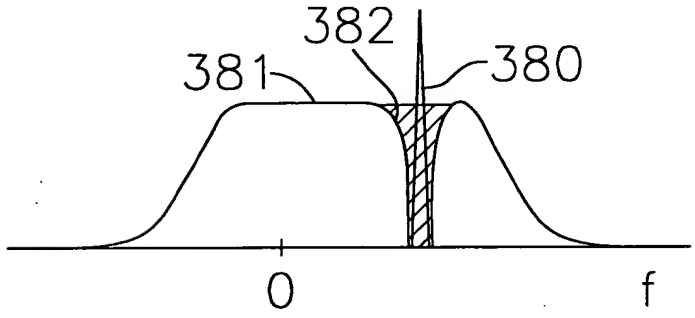


FIG.88C

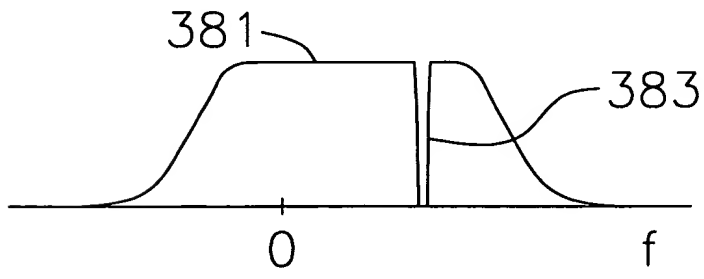


FIG.89A

16-QAM CONSTELLATION
BEFORE NOISE REJECTION

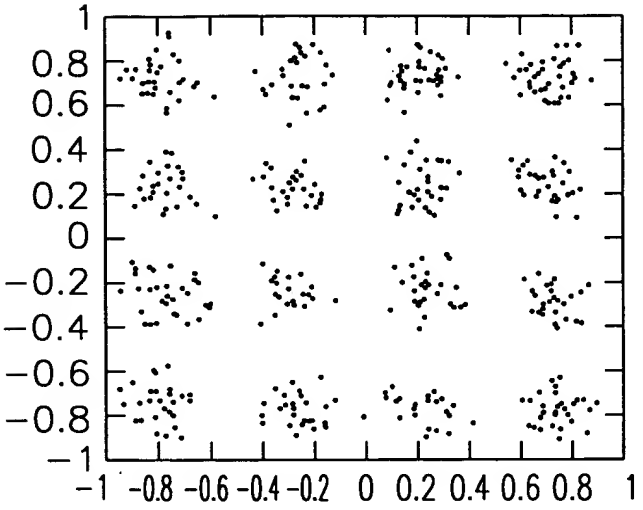


FIG.89B

16-QAM CONSTELLATION
AFTER NOISE REJECTION

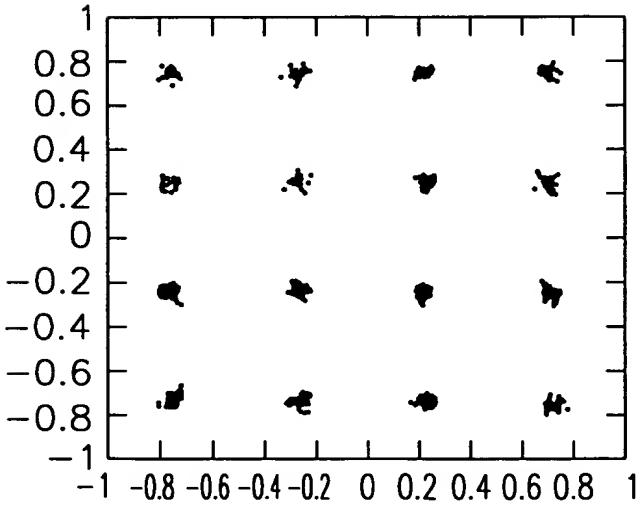


FIG. 90A

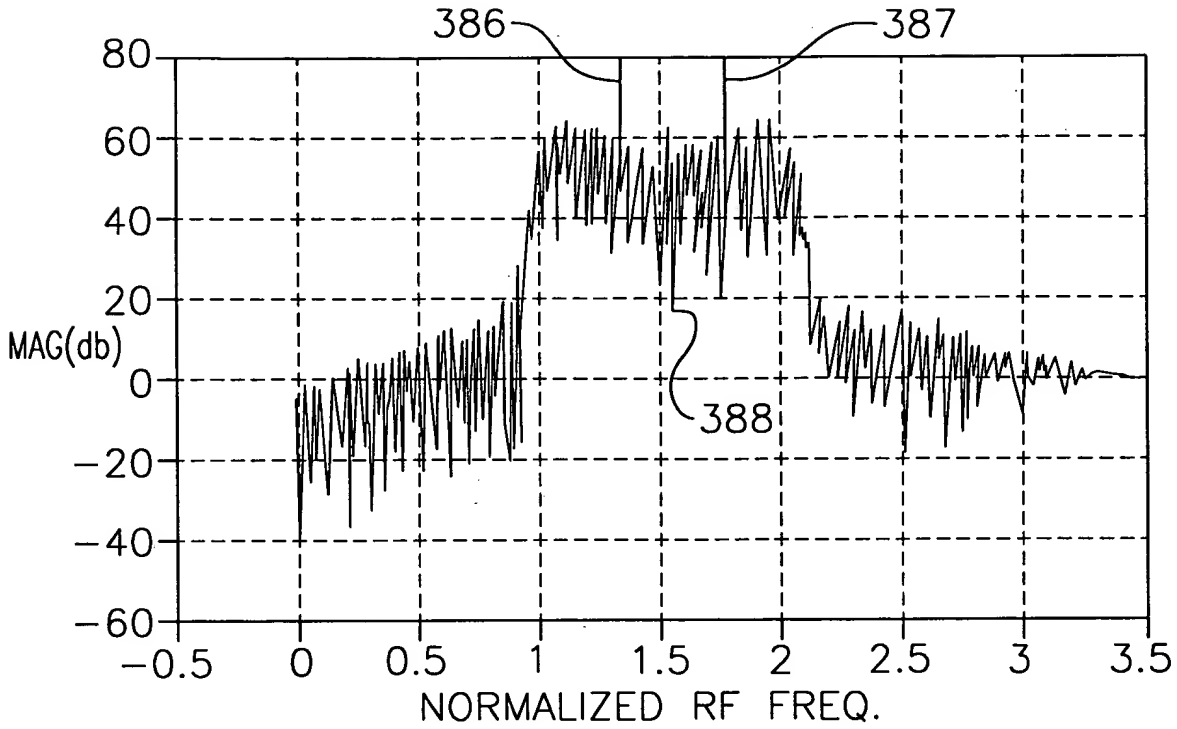


FIG. 90B